cadence®

# Modus Test Solution

## Reduce test time by up to 3X without impact to fault coverage or chip size

The Cadence® Modus™ Test Solution is a comprehensive next-generation physically aware design-for-test (DFT), automatic test pattern generation (ATPG), and silicon diagnostics tool. Using the Modus Test Solution, you can experience an up-to-3X reduction in test time using its patent-pending physically aware 2D Elastic Compression architecture, without any impact on fault coverage or chip size.

## Features and Benefits

### DFT logic insertion

- **New patent-pending physically aware 2D Elastic Compression architecture**
- **Compression ratios beyond 400X with up to a 3X reduction in test time and no impact on chip size or fault coverage**
- **Up to 2.6X reduction in compression logic wire length at 100X compression ratio**
- Programmable memory built-in self-test (PMBIST) with diagnostics, redundancy analysis, and soft and hard repair
- Shared test access bus for at-speed PMBIST across multiple embedded memories
- Logic built-in self-test (LBIST) with flexible two-pin direct-access or JTAG interface control
- Timing-aware test point insertion (TPI) for both increased fault coverage ramp and increased fault coverage
- IEEE 1149.1 and 1149.6 boundary scan
- Full and partial scan, XOR and broadcast/Illinois style decompression, XOR and MISR compression with X-masking
- Low pin-count test (LPCT) SmartScan compression (ideal for multi-site testing)
- Ultra LPCT using only two pins (ideal for analog/mixed-signal designs)
- Logical and physically aware scan-chain stitching
- IEEE 1500 wrapper core test
- IEEE 1687 embedded instrument compliant test access and pattern migration
- On-product clock generation (OPCG) and insertion for at-speed transition defect testing
- Common Power Format (CPF) and IEEE 1801-aware test with flexible power test access module (PTAM) control to enable manufacturing test in different power states and power domain crossing fault detection
- 2.5/3D stacked die wrapper and JTAG control with serial/parallel test access mechanism for die-level and inter-die test
- Automatic SDC generation for all DFT-related timing modes to enable faster timing closure

### Test pattern generation

- Unified TCL scripting and debug environment with Cadence's Genus™ Synthesis Solution, Innovus™ Implementation System, and Tempus™ Timing Signoff Solution
- Static, IDDQ, and I/O parametric fault models
- Timed (SDC and SDF) delay, small delay, and physically aware bridge fault models
- RAM sequential test
- Patented user-defined fault models
- Cell-aware fault modeling with Cadence Spectre™ simulators and Cadence Virtuoso® Liberate™ solutions
- Hierarchical SoC test pattern creation and migration leveraging IEEE 1500 and 1687 networks
- Distributed ATPG with near-linear runtime scalability across multiple machines and CPUs

- Powerful test mode and test logic data model with extensive Tcl-based query and reporting commands
- Low-power ATPG with scan and capture toggle count limits

### Silicon diagnostics and trend analysis

- Powerful single-pass multi-device precision diagnostics accelerates turnaround time by 20X
- Single-pass diagnosis of all supported compression architectures, including XOR, MISR, SmartScan, and 2D Elastic
- Integration with OpenAccess (OA) to enable physically aware diagnostic callouts and cross-probing between the logical schematic and the Virtuoso layout editor
- Integration with Cadence DFM pattern analysis to enable root-cause failure analysis
- Volume analysis tools and methods to identify critical-yield limiters enabling faster yield ramp

## 2D Compression

Scan compression logic forms a physically aware two-dimensional grid across the chip floorplan. The **Modus 2D Compression**'s grid structure consumes up to 2.6X less routing resources than traditional "one-dimensional" XOR compression circuits at a 100X compression ratio. Furthermore, the 2D grid structure scales sub-linearly with the compression ratio and at a 400X compression ratio is still no worse for routing resources than the traditional 1D XOR compression at only 100X.

## Elastic Compression

Registers and sequential feedback loops are interwoven with XOR logic in the decompressor circuit. The sequential nature of this circuit enables **Modus ATPG** to leverage multiple shift cycles to control register values in a single fault-capture cycle. Modus ATPG can also adaptively increase the number of shift cycles in a test pattern to be larger than the scan-chain length to provide yet more controllability to detect tough faults. **Modus Elastic Compression** is able to achieve compression ratios beyond 400X without any impact on fault coverage or fault diagnostics.

## Testpoint Insertion

Increasing fault coverage and reducing test time are two key benefits of the **Modus TPI** flow. With two distinct identification algorithms—deterministic fault analysis to improve coverage by targeting hard-to-test faults caused by high-care bit requirements, and random resistant fault analysis to reduce pattern count by targeting hard-to-test faults caused by resistance to random stimuli—Modus testpoints can effectively close your coverage and pattern count gaps. Tightly integrated into the Genus cockpit, Modus TPI is invoked by the Genus Synthesis Solution during the synthesis process—simplifying the flow for synthesis engineers who may be unfamiliar with TPI. This tight integration, coupled with comprehensive runtime controls, such as timing-driven slack-based testpoint selection, uniquely position Modus TPI to meet your testpoint needs.

## Volume Diagnostics

Analyzing a single silicon failure to root cause through physical failure analysis (PFA) can be very expensive and time consuming. So, to accelerate time to profitability, it's critical to select failing die that are the most statistically significant in terms of limiting yield ramp, which is where **Modus Diagnostics** volume analysis capabilities come in. Built on top of the Modus Diagnostics precision diagnosis engine, volume analysis leverages distributed processing and multiple defect diagnosis to enable fast diagnosis of a large number of failing die, and then loads these failures into a high-speed SQL database for further analysis. Once the database has been created, Modus Diagnostics volume analysis analyzes the failures for trends, and generates Pareto charts and wafer maps to identify the critical-yield-limiting failures. Silicon defects representing these limiting-defect classes can then be sent to PFA with confidence that the results of the analysis will improve yield fast.

## Low-Power Test

Effectively managing power consumption during silicon test is very critical. Testing at too low a power level means power-sensitive defects could be missed, while testing at too high a power level means the power grid or tester could be over-driven, resulting in false fails and yield loss. The Modus Test Solution offers **Modus ATPG**, a comprehensive low-power test solution starting with CPF and IEEE 1801 power-intent-driven DFT insertion in the Genus cockpit, coupled with Q-pin and clock gating to control test mode power. Modus ATPG low-power capabilities include both scan and capture toggle-rate controls, permitting the generation of a pattern set that strikes the right balance and most closely mimics functional power consumption at the tester.

## Mixed-Signal Test

Cadence is a long-standing leader in mixed-signal design, and is committed to the total interoperability of all of our tools through the OpenAccess database. **Modus DFT** natively integrates all DFT insertion with the Genus Synthesis Solution, which natively reads and writes OpenAccess. Since many mixed-signal designs are small, high-volume, low-margin catalog parts, Modus DFT offers low-pin-count test support (down to two pins) and SmartScan compression to address package and pin limits and enable scalable multi-site testing. To prevent X-sources from adversely affecting digital testing, automated IEEE 1500 wrapper insertion efficiently performs analog isolation. **Modus Diagnostics** is integrated with the **Virtuoso Layout Suite** via the OpenAccess database, enabling automated bridging fault-model generation critical to improving yield on high-volume devices, and logical-to-physical cross-probing during diagnosis to enable fast defect location visualization.

## Automotive Test

Automotive designs are growing aggressively in terms of size and complexity, and the ISO 26262 safety standard is demanding higher manufacturing test coverage (99.9%) and zero DPM—posing big challenges for automotive device designers. **Modus Logic BIST** combined with TPI is the perfect combination for meeting ISO 26262 demands. LBIST insertion and checking occurs natively in the Genus cockpit, simplifying the incorporation of LBIST including X-state blocking, and **Modus TPI** dramatically increases the LBIST coverage achieved during the short functional LBIST test cycles dictated by the safety standard. In addition, the Modus Test solution's flexible fault modelling enables a variety of defect modeling methodologies to minimize DPM, including cell-internal, gate-exhaustive, cell-aware, and bridging defect modelling. Memory BIST (MBIST), IEEE 1500 support, and a broad compression portfolio round out the complete Modus Test solution for the automotive segment.

## Platforms

- Linux (64-bit)
- IBM AIX (64-bit)

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information please visit: www.cadence.com/support-and-training

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