Genus Synthesis Solution

Massively parallel RTL synthesis and physical synthesis

In the complex world of chip design, you're constantly pushing to improve your chip—to get more performance, lower power, and improved area. Developing the best solution requires high accuracy and correlation, as well as extremely rapid turnaround time. To remain competitive, you can't afford to degrade any of these parameters—power, performance, area, accuracy, or runtime. With the Cadence® Genus™ Synthesis Solution, no compromises are necessary: you get the best and most highly correlated results in the shortest time.

Overview

The Genus Synthesis Solution is a next-generation RTL synthesis and physical synthesis tool that delivers up to a 10X boost in RTL design productivity with up to 5X faster turnaround times.The solution can scale its capacity to well beyond 10 million instances flat. It also delivers tight timing and wirelength correlation to within 5% of place and route.

Using the Genus Synthesis Solution, you can experience a 2X or more reduction in iterations between block-level and unit-level synthesis. In addition, you can achieve up to a 20% reduction in datapath area without any impact on performance.

Key Features and Benefits

- Massively parallel architecture works seamlessly over multiple machines and multiple CPUs per machine; delivers up to 5X faster runtimes with linear scalability beyond 10M instances flat
- Automatic extraction of full timing and physical contexts for any subset of a design; reduces iterations between unit-level and chip-/block-level synthesis by 2X or more
- Global analytical micro-architecture optimization delivers up to 20% reduction in datapath area without any impact on performance
- Unified GigaPlace™ engine, delay calculation, parasitic extraction, and timing-driven global routing with the Cadence Innovus™ Implementation System; timing and wirelength between the tools correlate to within 5%
- Unified next-generation user interface with the Innovus Implementation System and Cadence Tempus™ Timing Signoff Solution
- Physically aware logic structuring and mapping
- Power domain and layer-aware net buffering
- Single-pass multi-Vt optimization

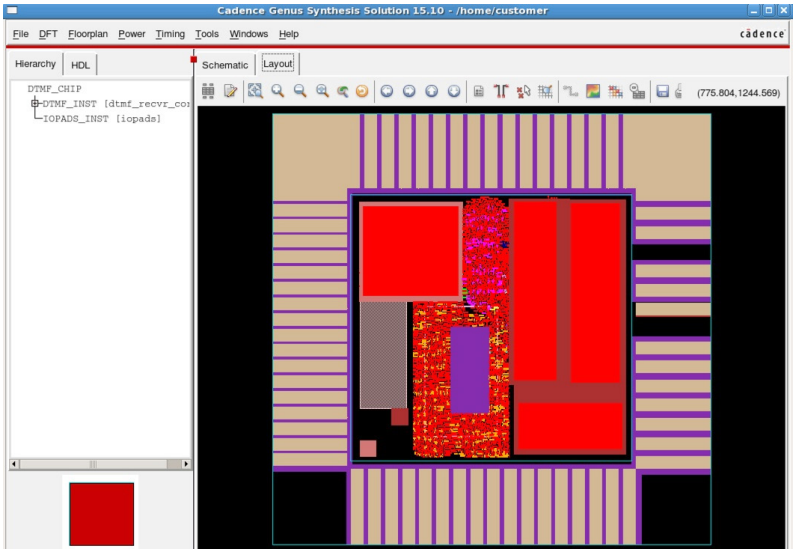

Figure 1: The Genus Synthesis Solution enables timing debug with physical interconnect knowledge built-in. Cross-probe to the physical viewer to see associated wirelengths, floorplan blockages, and estimated routing, and extract the chip-/block-level physical context for use in unit-level RTL design.

- Hierarchical RTL register clock gating
- Timing-driven physically aware multi-bit flop mapping
- Pipeline and general register retiming
- ChipWare functional components and simulation models
- Full support for multiple power domain design with automatic low-power cell insertion, both CPF and IEEE 1801 power-intent specifications supported
- Concurrent MMMC timing analysis and optimization
- Native integration of all design for test (DFT) logic insertion
- Verilog 1995 and 2001, System Verilog 1800-2009, and VHDL 1987, 1993, and 2008 input formats
- Verilog netlist and DEF placement output formats, Innovus database output format also supported
- Multi-bit cell insertion to group registers for power and area reduction

Massively Parallel Architecture

The Genus Synthesis Solution is built on a new massively parallel architecture that performs distributed synthesis across multiple machines and CPUs. It leverages a proprietary, timing-driven partitioning algorithm that slices transparently across design hierarchy and evenly distributes the optimization effort across different machines. All told, this architecture enables the solution to deliver up to 5X faster synthesis turnaround times with linear scalability to well beyond 10 million instances.

Physically Aware Context Generation

A simple Tcl command at the end of a chip- or block-level synthesis can be used to "clip" out the full timing and physical context for any subset of a design. These clips can be used to drive unit-level RTL synthesis with full consideration of chip- or block-level timing, floorplan, and placement. By using these clips, you can experience a 2X or more reduction in unit-level iterations required to achieve timing closure.

Tight Correlation to Place and Route

The Genus Synthesis Solution shares several common engines with the Innovus Implementation System, including the GigaPlace engine, delay calculation, parasitic extraction, and timing-driven global routing. Timing and wirelength between the tools correlate tightly to within 5%, and global routing performance is 4X better. Both tools are critical for productivity at advanced nodes such as 7nm and below.

Architecture-Level PPA Optimization

A new, proprietary algorithm identifies critical datapath regions in a design, regardless of their physical or logical module hierarchy. For each of these regions, the Genus Synthesis Solution considers a number of possible microarchitectures with different power, performance, and area (PPA) tradeoffs. It then builds and solves an analytical model over all datapath regions to achieve the globally best PPA for the design. This technology can reduce datapath area by up to 20% without any impact on performance. Deep datapath applications, such as machine learning processors, benefit the most from this technology.

CPF and IEEE 1801 Support

The Genus Synthesis Solution includes extensive capabilities to support complex multi-power domain designs. Power-intentpecifications can be provided in either CPF or IEEE 1801 formats, with the solution performing full automatic insertion of level shifters, isolation cells, and retention elements. Always-on buffering and power domain-aware routing are also fully supported.

Power Optimization

To reduce power consumption, the solution features a comprehensive range of techniques, including timing and physically aware multi-bit flop mapping, hierarchical RTL clock gating, and intelligent one-step use of multiple threshold cell libraries during mapping and optimization.

Register Retiming

The Genus Synthesis Solution can retime registers along pipelines and around sequential loops. Retiming can increase or decrease the number of flops along the retiming cut to achieve the best possible PPA tradeoff.

ChipWare Components

The solution includes a complete portfolio of industry-standard functional building block components such as fixed-point arithmetic, floating-point arithmetic, and pipeline units. Simulation models are also included for all ChipWare components.

DFT

With the Genus Synthesis Solution, you get natively integrated full support for design for test (DFT), including timing-driven physically aware scan chain stitching and insertion of compression logic, memory BIST, logic BIST, JTAG, on-product clock generation (OPCG), and power test access module (PTAM) logic. The Genus Synthesis Solution's native integration of the Cadence Modus DFT Software Solution gives the only working solution for the routing congestion from high scan compression ratios using 2D Elastic Compression.

Safety Critical and Automotive

The Genus Synthesis Solution is part of the industry's first comprehensive "Fit for Purpose - Tool Confidence Level 1 (TCL1)" certification from TÜV SÜD, enabling automotive semiconductor manufacturers, OEMs, and component suppliers to meet stringent ISO 26262 automotive safety requirements. To achieve certification, Cadence provided its tool and flow documentation to TÜV SÜD for evaluation, and TÜV SÜD confirmed the Cadence flows are fit for use with ASIL A through ASIL D automotive design projects. Cadence customers can easily access the tool and flow documentation and TÜV SÜD technical reports via the Cadence Automotive Functional Safety Kits at www.cadence.com/go/iso26262cert.

Common UI for Ease of Use

The Genus Synthesis Solution has a common UI with the Innovus Implementation System and the Tempus Timing Signoff Solution. The system simplifies command naming and align common implementation methods across these Cadence digital and signoff tools. For example, the processes of design initialization, database access, command consistency, and metric collection have all been streamlined and simplified. In addition, updated and shared methods have been added to run, define, and deploy reference flows. These updated interfaces and reference flows increase productivity by delivering a familiar interface across core implementation and signoff products. You can take advantage of consistently robust RTL-to-signoff reporting and management, as well as a customizable environment.

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

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