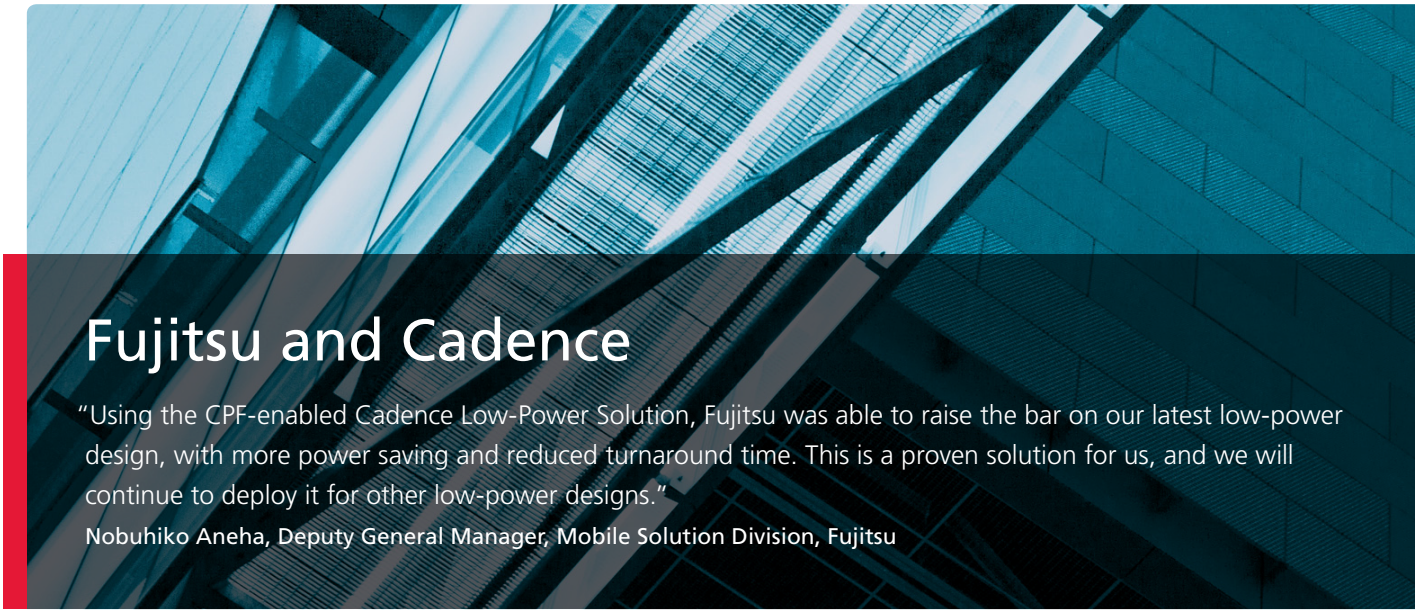
cadence®



Fujitsu and Cadence

"Using the CPF-enabled Cadence Low-Power Solution, Fujitsu was able to raise the bar on our latest low-power design, with more power saving and reduced turnaround time. This is a proven solution for us, and we will continue to deploy it for other low-power designs."

Nobuhiko Aneha, Deputy General Manager, Mobile Solution Division, Fujitsu

The Customer

Mobile phones continue to grow exponentially in bandwidth requirements due to advances in multimedia offerings and consumer demand. In fact, handheld mobile devices are projected to approach the bandwidth consumption of cable or DSL. One new technology option to meet these needs is microwave, which offers new frequencies, higher data rates, and longer reception ranges from the base station. Over the past five years, industry leaders have developed a new standard for Worldwide Interoperability for Microwave Access (WiMAX).

Fujitsu Microelectronics Limited, a global leader in microelectronics for computers and communications devices, has now successfully developed the first 65nm SoC for mobile WiMAX applications. This fully integrated MAC and PHY mixed-signal baseband processor is designed to support frequencies ranging from 2 to 11GHz in both licensed and unlicensed bands.

The Challenge

The key to mobility and submicron success is optimizing the power design for the lowest possible overall usage and shutoff leakage.

Previously, independent decisions would be made at each stage of the design process, many of which would impact other areas in unforeseen ways and adversely affect the final power characteristics.

Business Challenge

- Make mobile WiMAX a reality by reducing chip size and power requirements

Design Challenges

- Align power design around CPF with accurate simulation
- Move to smaller geometries
- Reduce design time and improve quality of silicon

Cadence Solutions

- Low-Power Solution
- Encounter Digital Implementation System
- Incisive Design Team Simulator
- Encounter Conformal Low Power

Results

- Reduced leakage power by 88% and overall power consumption by 36%
- Reduced physical design turnaround time by 50%
- Accurate verification of final design improves silicon quality

The Solution

Now, a more unified approach to applying reference specifications from the beginning of the design process drives optimization across engineering specializations to achieve the lowest power overall levels in the final product. This Common Power Format (CPF)-enabled Cadence® Low-Power methodology is becoming an important part of the reference design flow (RDF) mechanism for low-power, submicron system-on-chip (SoC) designs.

In 2007, Fujitsu developed its own CPF-based RDF concept for the WiMAX project. Reducing overall power requirements was a major hurdle in the development of mobile WiMAX devices that other consortiums had not been able to overcome.

For the main design flow of this project, Fujitsu chose the Cadence Low-Power Solution, which provides full front-to-back low-power capabilities for design, verification, and implementation. The Fujitsu RDF implementation was built around the Cadence platform to ensure smooth integration and data handoffs. Many CPF innovations were also incorporated into the Low-Power Solution and the Cadence Encounter® Digital Implementation System, creating the most advanced turnkey platform for CPF-enabled low-power design.

"Being able to work directly with the Cadence team to adapt and refine our own developments was an important part of the success of this project," explains Nobuhiko Aneha, Deputy General Manager of the Mobile Solution Division at Fujitsu Microelectronics Limited.

Utilizing this global design system, Fujitsu achieved results that surpassed the original design targets, reducing leakage power levels in the design by 88%, and reducing overall chip power consumption by 36%.

In addition to the benefits of CPF, the automated power shutoff (PSO) flow in the Encounter Digital Implementation System reduced Fujitsu's physical design turnaround time by about 50%.

"The integration of the Cadence solution improved performance and helped us to shorten our development schedule. This is critical to establishing our competitive edge in this emerging standard," Aneha says.

The CPF-based Cadence Incisive® Design Team Simulator enabled Fujitsu to run logic simulations for the power shutoffs in the design without the need to create a custom programming language interface (PLI).

Encounter Conformal® Low Power provided structural and functional verification to identify low-power design rule oversights. Further verification using Incisive Design Team Simulator and Conformal Low Power contributed to improved quality of silicon (QoS) in the final output.

Summary and Future Plans

Cadence anticipates increasing demand for CPF-enabled techniques, and has incorporated these advances across the Low-Power Solution platform. This technology has now been proven to improve performance, increase productivity, and speed time to market on real production designs in global companies like Fujitsu.

Power-management strategies—such as multi-supply multi-voltage (MSMV), dynamic voltage and frequency scaling (DVFS), and power shutoff (PSO)—increase the complexities of the design. The ability to perform more comprehensive "what if" analyses early in the design cycle improves the efficiency of these power-saving techniques, while reducing the risks of ad hoc solutions and dramatically increasing productivity.

Applying optimization engines later in the design flow can fine-tune the tradeoffs among timing, power, and area requirements. Finally, with direct impact on budgets and time to market, the integrated Cadence logic design, verification, and implementation technologies accurately model the product to reduce the number of iterations in the design flow and improve the quality of the first silicon.