Pattern-based analytics to estimate and track yield risk of designs down to 7nm

JASON CAIN, MOUTAZ FAKHRY (AMD)
PIYUSH PATHAK, JASON SWEIS, PHILIPPE HURAT, YA-CHIEH LAI
(CADENCE)
INTRODUCTION

Layout pattern matching engines have been available in the IC physical design ecosystem for over a decade.

The use of pattern matching to augment design-rule checking (DRC) in the physical verification flow has been widely adopted since the 32/28nm generation.

The more recent introduction of topological-based pattern matching engines has opened a range of new applications for layout analysis.

- Pattern cataloging can be used to identify all unique pattern topologies (with or without specific dimensions) in a layout.
- Catalogued pattern topologies can be compared between layouts to identify differences and commonalities and to identify potential risks.
A powerful tool for characterizing and comparing physical designs
Compact form for describing patterns
Can be independent of physical dimensions
1. Systematically scan a window across entire design (choice of window size is important!)

2. In every window, break-down and identify every pattern and sub-pattern that exists in that design (with dimensions)

3. Store a full catalog of all patterns with dimensions
TOPOLOGICAL PATTERN EXAMPLES FOR MX LAYERS
14NM DIGITAL LOGIC – WINDOW SIZE = 3 METAL PITCHES

3x3

6x6

10x10
The same circuit was implemented in 28, 20, 14, and 7 nm technologies.

Pattern extraction was run on each and the number of unique topologies was counted.

Note the use of a log scale.

### Technology Node | Total Unique Topologies | Total Exact Patterns
--- | --- | ---
28 nm | 20,763,677 | 286,593,810
20 nm | 835,025 | 39,977,934
14 nm | 242,633 | 17,634,752
7 nm | 4,964 | 197,257
Let's take a closer look at those 7nm patterns

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>Capture Layer</th>
<th>Capture Max Window</th>
<th>Total Unique Topologies</th>
<th>Total Exact Patterns</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 nm</td>
<td>1x metal</td>
<td>3 pitch (7nm 1x metal rules)</td>
<td>4,964</td>
<td>197,257</td>
</tr>
</tbody>
</table>

- Only a small number of topologies contribute to the vast majority of patterns
- There is still a long tail of topologies with small number of pattern variants (though much better than at older nodes)
- Looking more closely at the top 1231 topologies that contribute 95.45% of all exact patterns
- For comparison at 14nm, 23,056 topologies (out of 242,633) contribute 95.45% of all exact patterns
WHAT DOES IT MEAN FOR A TOPOLOGY TO HAVE MULTIPLE EXACT PATTERNS?

- This is our most common topology
- There are 3061 exact pattern variants of this topology
- All the variation is along the x dimension of this pattern!

- This is an example of a topology with only a single corresponding exact pattern
- Design rules only yielded a single exact variant in design!
TOPOLOGY AND PATTERN COUNT STATISTICS

7NM MOL/BEOL LAYERS

Counts-Topo  Counts-Pattern
VIA ANCHORED PATTERNS
EVOLUTION OF COMPLEXITY ACROSS 14/20NM STACK

**14NM**

- V1/M1
- V1/M2
- V2/M2
- V2/M3

**20NM**

- V1/M1
- V1/M2
- V2/M2
- V2/M3

Compared to 14nm, 20nm Vx/Mx patterns have a longer range towards the low complexity bins.

Compared to 20nm, 14nm complexity bin coverage shows minor reduction in max scanlines.
VIA ANCHORED PATTERNS
EVOLUTION OF COMPLEXITY ACROSS 7NM STACK

CA.M0
V0.M0
V0.M1
V1.M1
V1.M2
V2.M2
V2.M3

Mx layer represents wafer design intent shapes.
Topological complexity of patterns is highest for V1.M1 and V0.M1 patterns among Mx/Vx layers.
AM.M3, V1.M2, and V2.M2 have the most variability (average) in terms of patterns per signature across the BEOL stack.
V1.M1 has the largest coverage of complexity bins.
- It is attributed to line-end (cut shapes) and via densities per pattern.
Routed Mx layer patterns V1.M2, V2.M2, and V2.M3 show mostly single complexity bin of 9 covered by most patterns in one direction.
- This is due to the maximum number of unidirectional metal tracks covered per pattern.

10x11
17x14

pattern.
Overall goal is to identify critical new patterns introduced into new designs (Target) compared to existing design(s) (Baseline).

Reasonable runtime: Minutes for differencing, hours for search.

Tools and flow scale easily to a billion patterns.

Implemented analytics and scoring function to identify set of yield-limiting candidate patterns.
7NM VS. 14NM/20NM – COMMON METAL LAYERS

TOPOLOGIES AND PATTERNS

~55% signatures (for 7nm block) are new.

~92% patterns (for 7nm block) are new!
PATTERN ANALYTICS AND SCORING:

COMPLEXITY

Complexity: $C_{xy} = C_x \times C_y = 9 \times 10 = 90$
PATTERN ANALYTICS AND SCORING:
COUNT OF CRITICAL DIMENSIONS (CCD)

• Count of critical dimensions
  – Line-ends
  – Inner corners
  – Space/Width
  – Island shapes: includes –
    – Rect., U, L, Z, T with min-area

Pattern
ccd = 16

ccd-lineEnds = 2
ccd-space = 3
ccd-width = 6
ccd-innerCorner = 5
Pattern Analyses

$\textit{Counts of critical dimensions (DFM metric)}$

\[ f(\text{ccd,Cxy}) = \text{Score} \rightarrow \]

Validation: Simulation Hotspot Coverage

Hotspot coverage by scored bin

% of defect patterns by score bin

\[ \% \text{ of patterns with defect by score bin} \]
EXAMPLES OF WEAK LITHO HOTSPOTS ON 2X METAL LEVELS

2X Metal PW necking at Dense-ISO transition
By maintaining a master database of layout topologies and patterns, each new design can be compared with all previous designs.

Potentially problematic patterns can be identified before silicon:
- Monitor on target product
- Consider removing from future designs
Previous pattern cataloging work was extended to 7nm and the trend toward lower layout complexity continues.

Pattern-based analysis of 7nm metal stack was completed

Analysis at 7nm suggested that there is some signal to identify risky patterns based on pattern features

Preliminary analysis of pattern features shows some correlation with simulated process risk

Future work includes evaluating tradeoffs in DFM layout optimization and layout complexity
The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions and typographical errors.

The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

AMD MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION.

AMD SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD BE LIABLE TO ANY PERSON FOR ANY DIRECT, INDIRECT, SPECIAL OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD IS EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

ATTRIBUTION

© 2016 Advanced Micro Devices, Inc. All rights reserved. AMD, the AMD Arrow logo and combinations thereof are trademarks of Advanced Micro Devices, Inc. in the United States and/or other jurisdictions. Other names are for informational purposes only and may be trademarks of their respective owners.