SiFive Tapeout 7nm/12nm/14nm Products Using Cadence Tempus™ ECO and Signoff

Challenges Solved
• Finding fastest path to custom silicon
• Meeting challenging clock structures, aggressive project schedules, and leakage power recovery challenges on advanced-node 100M+ instance designs

Benefits
• Achieve PPA faster due to better correlation between Cadence® Innovus™ Implementation System and Tempus™ Timing Signoff Solution
• Reduced iterations with P&R flow and leakage power recovery of ~ 8% with Tempus ECO
• Reduced project turnaround time by 1.3X with Tempus ECO and Signoff flow
• Very predictable and physically aware ECO turnarounds

Design
• Networking/AI/CPU/CPU-subsystem/storage chips designs at advanced nodes

Parthasarathy Narasimhan, Sr. Director, ASIC Design Engineering