Open-Silicon
Your Idea. Delivered.™
a SiFive company

"We trust the Cadence Tempus Timing Signoff Solution as our timing tool of choice for all of our SoCs across applications on satellite systems, aerospace control systems, SSD controllers, satellite beamforming, USB products, AI products, RISC-V, and machine learning SoCs. Its performance, coupled with integration within the Cadence Innovus Implementation System, has allowed us to significantly reduce the time we spend in timing closure and achieve better PPA. The size and complexity of our designs, some in the range of ~130M instances, require timing ECOs to be handled efficiently and the Tempus solution was the right timing platform to address our needs. Furthermore, by using the Tempus solution for signoff, we are able to converge and achieve faster design closure time."

Parthasarathy Narasimhan,
Sr. Director, ASIC Design Engineering

CUSTOMER SUCCESS

SiFive Tapeout 7nm/12nm/14nm Products Using Cadence Tempus™ ECO and Signoff

Challenges Solved

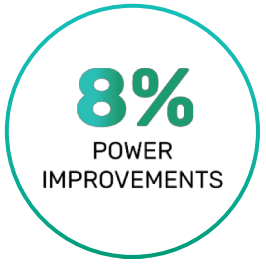
- Finding fastest path to custom silicon
- Meeting challenging clock structures, aggressive project schedules, and leakage power recovery challenges on advanced-node 100M+ instance designs

Benefits

- Achieve PPA faster due to better correlation between Cadence® Innovus™ Implementation System and Tempus™ Timing Signoff Solution
- Reduced iterations with P&R flow and leakage power recovery of ~ 8% with Tempus ECO
- Reduced project turnaround time by 1.3X with Tempus ECO and Signoff flow
- Very predictable and physically aware ECO turnarounds

Design

- Networking/AI/CPU/CPU-subsystem/storage chips designs at advanced nodes



cadence®