METHODOLOGY FOR ANALYZING AND QUANTIFYING DESIGN STYLE CHANGES AND COMPLEXITY USING TOPOLOGICAL PATTERNS

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\textsuperscript{1}ADVANCED MICRO DEVICES, \textsuperscript{2}CADENCE DESIGN SYSTEMS
Pattern matching engines have been available in the IC physical design ecosystem for over a decade.

The use of pattern matching to augment design-rule checking (DRC) in the physical verification flow has been widely adopted.

Early pattern matching engines used a three-value logic (TVL) method for describing patterns.

The more recent introduction of topological-based pattern matching engines has opened a range of new applications for layout analysis.
TOPOLOGICAL PATTERN DESCRIPTION

The “3-finger” Pattern

Deltas and Scanlines

Bit Pattern

- A powerful tool for characterizing and comparing physical designs
- Compact form for describing patterns
- Can be independent of physical dimensions
TOPOLOGICAL PATTERNS CAN BE USED FOR ANALYSIS

1. Understand usage of patterns in your designs (with locations)
2. Identify common cases (which must yield well) and outliers/edge cases
3. **Identify what is new/different in an incoming design**
LAYOUT PATTERN EXTRACTION

1. Systematically scan a window across entire design (choice of window size is important!)

2. In every window, break-down and identify every pattern and sub-pattern that exists in that design (with dimensions)

3. Store a full catalog of all patterns with dimensions

Pattern Capture

- Reference Design(s) (OASIS,GDS)
- Pattern Extraction
- Database of Known Patterns/Dimensions

- In our experiments, full chip 1X Metal layers captured in < 8 hours w/ 32 CPUs
TOPOLOGICAL PATTERN EXAMPLES FOR MX LAYERS
14NM DIGITAL LOGIC – WINDOW SIZE = 3 METAL PITCHES

3x3

6x6

10x10
PATTERN EXTRACTION FOR 14NM DIGITAL LOGIC
1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES, INEXACT MATCHES
The same circuit was implemented in 28, 20, and 14 nm technologies.

Pattern extraction was run on each and the number of unique topologies was counted.

- Note the use of a log scale.

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>Total Unique Patterns</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 nm</td>
<td>20,718,038</td>
</tr>
<tr>
<td>20 nm</td>
<td>835,017</td>
</tr>
<tr>
<td>14 nm</td>
<td>242,617</td>
</tr>
</tbody>
</table>
EVOLUTION OF DESIGN TOPOLOGICAL COMPLEXITY
1X METAL LAYERS, WINDOW = 3 METAL PITCHES, INEXACT MATCHES

An order of magnitude decrease in the design complexity (as measured by the number of unique topologies) of 1x metal layers from 28nm to 20nm.
- Shift to double patterning
- Some metal routing complexity shifted to local interconnect

Additional decrease of ~4× from 20nm to 14nm despite the fact that 1x metal design rules are very similar.
- Shift to FinFET devices and impact of increased regularity of front end
DISTRIBUTION OF TOPOLOGY COUNTS
14NM DIGITAL BLOCK, 1X METAL LAYERS

Pattern Count vs. Pattern Index graph with a logarithmic scale.
### PATTERN SPACE SIZE

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>Total Possible</th>
<th>Reduced Space*</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3</td>
<td>512</td>
<td>38 (7%)</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>4,096</td>
<td>299 (7%)</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>32,768</td>
<td>1,716 (5%)</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>262,144</td>
<td>9,044 (3%)</td>
</tr>
<tr>
<td>3</td>
<td>7</td>
<td>2,097,152</td>
<td>49,610 (2%)</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>16,777,216</td>
<td>267,390 (2%)</td>
</tr>
<tr>
<td>3</td>
<td>9</td>
<td>134,217,728</td>
<td>1,452,652 (1%)</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>1,073,741,824</td>
<td>7,864,304 (1%)</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>65,536</td>
<td>1,900 (3%)</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>1,048,576</td>
<td>43,428 (4%)</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>16,777,216</td>
<td>479,491 (3%)</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>268,435,456</td>
<td>5,202,792 (2%)</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>33,554,432</td>
<td>500,948 (1%)</td>
</tr>
</tbody>
</table>

*Reduced space removes duplicates due to rotation or mirroring and non-physical patterns.

- The number of possible patterns in each topological family grows very rapidly with topological complexity.
Despite the highest raw count of unique patterns occurring for pattern topologies in the 6×7 family the coverage of the total pattern space is quite low in that region.

Pattern coverage near 100% for basic topologies (3×3) but drops off quickly.
IDENTIFICATION OF LAYOUT DIFFERENCES

How do we define what is “new”?  
1. **Topologically Different:** Patterns that have never been seen before  
2. **Dimensionally Different:** Patterns whose dimensions are outside the range of what has been seen before

Use cases

1. Identify regions where customer has modified sensitive IP  
2. Give OPC engineers regions that need more analysis  
3. Feed forward monitoring points to process teams and FA  
4. Give entire team an indication of how difficult a new tape-out will be, especially ramping up a new process
HOW CAN WE IDENTIFY WHAT IS “NEW” IN AN INCOMING DESIGN THAT WE HAVE NEVER SEEN BEFORE?

Pattern Capture

Reference Design(s) (OASIS,GDS) → Pattern Extraction → Database of Known Patterns/Dimensions

Pattern Compare

New Design (OASIS,GDS) → Identify Pattern Differences → What’s New?
AUTOMATIC IDENTIFICATION OF REPRESENTATIVE LAYOUT DIFFERENCES

Each red point is a representative pattern present only in new design

Pattern extraction target (digital block)
AUTOMATIC IDENTIFICATION OF REPRESENTATIVE LAYOUT DIFFERENCES

- Memory
- Different standard cell library
- Custom IP
- Pattern extraction target (digital block)
- Different router settings
TOPOLOGICAL DESIGN COMPARISON
1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES, INEXACT MATCHES

Same circuit design

Database of Topological Patterns

Comparison Engine

Database of Topological Patterns

N20

N14

677,486

157,539

85,094

14 nm

20 nm
Pattern matching results can drive actions to mitigate risk

- For patterns used frequently, notify the fab for monitoring and/or process optimization.
- For infrequent patterns, consider removing from the design.

Once patterns captured, comparisons performed in < 1 hour.

New topologies not validated on test chip!
COMPARISON OF PRODUCT DESIGN STYLES
1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES

Inexact matching

Exact matching
SUMMARY

- Topological pattern analysis provides powerful tools for measuring physical design complexity.

- Pattern extraction can be used to identify all unique pattern topologies (with or without specific dimensions) in a layout.
  - Measurable decrease in 1x metal design complexity from 28nm to 20nm to 14nm confirms that layouts are becoming more regular.

- Extracted pattern topologies can be compared between layouts to identify differences and commonalities.
  - May be used to identify potential risks and/or drive improved layout regularity.
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