Part of the Cadence® Virtuoso® Layout Suite family of products, Virtuoso Layout Suite GXL is a collection of automatic layout engines such as custom placement engines, routing, layout optimization, module generation, and analog/mixed-signal floorplanning. It supports the physical implementation of analog, custom-digital, and mixed-signal designs at the device, cell, block, and chip level. Built upon the connectivity- and constraint-driven layout environment of the Virtuoso Layout Suite platform, Virtuoso Layout Suite GXL ensures faster convergence on design goals and more efficient layout implementation.

Virtuoso Layout Suite GXL accelerates custom layout with a comprehensive set of user-configurable, easy-to-use pure polygon layout features within a fully hierarchical environment. Additional layout productivity is provided through optional parameterized cells (PCells) and SKILL®, the powerful scripting language that provides direct database access, tool configuration, and interoperability with other tools.

The industry leader in advanced custom layout automation, Virtuoso Layout Suite GXL offers a robust set of technologies for custom placement, routing, layout optimization, module generation, and analog/mixed-signal floorplanning. These technologies have revolutionized the way layout is generated, complementing hand-crafted layout with rich levels of automation that boost layout designer productivity by 2-20X.

Virtuoso Layout Suite GXL is built upon the fully featured connectivity- and constraint-driven environment that is at the core of the Virtuoso platform. Virtuoso Layout Suite GXL technologies can also be accessed from the Virtuoso Layout Suite EAD.

Virtuoso custom design platform, a complete solution for front-to-back custom analog, digital, RF, and mixed-signal design. The Virtuoso Layout Suite preserves design intent throughout the entire physical implementation process, while managing multiple levels of design abstractions from device, cell, and block levels through to the full-chip level.
It provides the fastest path to design convergence for mature and advanced node silicon realization.

The Virtuoso Layout Suite includes three tiers of increasing layout automation and designer productivity. By selectively automating aspects of custom-analog design and providing advanced technologies integrated on a common database, engineers can focus on precision-crafting their designs without sacrificing creativity to repetitive manual tasks.

In addition to Virtuoso Layout Suite GXL, the suite includes:

- **Virtuoso Layout Suite L**, a basic design-creation and implementation environment focused on layout productivity
- **Virtuoso Layout Suite XL**, an extension to the L tier, is built upon common design intent—the connectivity- and constraint-driven environment at the core of the Virtuoso platform

**Virtuoso Custom Design Platform**

The Virtuoso custom design platform integrates Virtuoso Schematic Editor, Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and the Virtuoso Layout Suite to speed convergence on design goals at every step for front-to-back custom analog, digital, RF, and mixed-signal design flows. The platform is backed by the largest number of process design kits (PDKs) available from the world’s leading foundries, for process nodes everywhere from mature 0.60um to advanced 7nm. It is built on the OpenAccess database, engineered by Cadence for industry-wide interoperability.

The Virtuoso custom design platform also interoperates with the Cadence Innovus™ digital implementation platform technologies via the OpenAccess database, providing a single, complete, coherent, and unified representation of mixed-signal design intent. This mixed-signal design intent is preserved throughout the entire physical implementation phase while operating with multiple levels of design abstractions (device, cell, block, chip), speeding design convergence to realize silicon for complex mixed-signal and system-on-chip designs.

**Virtuoso Layout Suite GXL Benefits**

The GXL configuration includes all Virtuoso Layout Suite L and XL features (see respective datasheets) and offers these additional benefits:

- **Virtuoso Floorplanner**: Supports soft- and hard-design abstracts for full-custom floorplanning of both block- and chip-level designs with innovative pin-optimization engine
- **Virtuoso Space-Based Router**: High-performance, high-capacity constraints-driven custom router for chip assembly, IP blocks, and/or custom digital designs with thousands of specialty nets
- **Pin-to-trunk routing**: New structured device-level routing capabilities in Virtuoso Space-Based Router can enhance routing productivity by as much as 50%
- **State-of-the-art wire editor**: Provides interactive and assisted automation wire and bus wiring
- **Module generation (ModGen)**: Generates complex interdigitating patterns, enhanced with new placement pattern editor and topology routing
- **Symbolic placement of devices**: A new device placement environment with smart symbolic display and smart flightlines that are all about speed
- **Virtuoso Digital Custom Placer**: Speeds up custom digital designs implementation for standard cell-based designs
- **Analog auto placer and cell planner**: A constraints-driven analog placer that is fully design-intent and design-rule aware

**Virtuoso Layout Suite GXL Features**

**Connectivity-driven functions and flow**

Virtuoso Layout Suite GXL changes the way custom block authoring is done. Driven by schematic connectivity and constraint design intent established in Virtuoso Schematic Editor or a netlist source (such as CDL or SPICE), an LVS-correct layout can be done in real-time. This ensures correct-by-construction layout, higher productivity, and shorter verification time. Additionally, tedious design tasks can be automated, such as device generation, placement, and routing. Schematics and layout can be cross-probed to highlight instances and devices as well as quickly identify unconnected nets.

In Virtuoso Layout Suite GXL, a new incremental connectivity-driven binding technology has been introduced. This approach is far superior to traditional name-based schematic-to-layout binders, which had severe limitations when supporting schematic-to-layout name mismatches. The connectivity-driven binder enables better support of legacy layouts that have name mismatches, and also improves handling of engineering change orders (ECOs) that involve renaming of instances and terminals in the layout. The incremental nature of the connectivity binder also greatly improves the performance of a connectivity-driven layout flow.

**Constraint- and design-rule-driven functions**

The Virtuoso platform is built upon a common constraint environment to ensure correct-by-construction layout, higher productivity, and fewer physical verification iterations. Topological constraints, electrical constraints, and/or design-rule specific constraints complete the design intent specified and managed in Virtuoso Schematic Editor, Virtuoso Analog Design Environment, or Virtuoso Layout Suite. Simply set the design intent constraints in Schematic Editor and Layout Suite can easily be configured to either enforce the constraints while generating layout
or automatically flag and log constraint violations that can be discussed at subsequent design reviews.

Integrated signoff constraint verification can be run and accessed from the docked annotation browser, simplifying the task of verifying that a design is meeting the design intent specification. Constraint verification can be done before, during, or after physical implementation of a design.

Symbolic placement of devices
Symbolic placement of devices is a new innovative transistor-level placement-planning environment that combines symbolic display, row-based placement, smart editing features, and smart flightlines for visualizing routing complexity.

Using the smart symbolic display, users can focus on the most relevant information needed to complete the task while abstracting unneeded data elements from the layout canvas. This new placement methodology can save up to 50% of the layout time.

State-of-the-art wire editor
Virtuoso Layout Suite GXL has a robust set of interactive and assisted wire-editing capabilities. This comprehensive wire editor is natively integrated into Virtuoso Layout Suite GXL utilizing the Virtuoso Space-Based Router technology. It has support for an array of specialty routing types such as bus/bundle, differential pair, matched length, and symmetry, and is fully enabled on all processes nodes including the most advanced process technologies.

In addition, users can take advantage of the wire editor’s assisted capabilities. Commands such as point-to-point, finish wire, pushing and shoving of wires, along with guided routing on single nets and buses, are built upon the Virtuoso common constraint system and connectivity-driven layout.

Virtuoso Space-Based Router
Virtuoso Space-Based Router is a hierarchical, space-based, full-chip, block- and device-level routing system for advanced analog, mixed-signal, and custom-digital designs. It has been used in production design of the most advanced process nodes. The routing environment is native to Virtuoso Layout Suite GXL and is tightly coupled with the Virtuoso common constraint environment. It is a multi-threaded routing environment, capable of routing multimillion-net designs.

Virtuoso Space-Based Router also supports a robust set of specialty custom routing constraints such as bus/bundle, differential pair, pin-to-trunk, match length, and shielding. A new pin-to-trunk routing use model of Virtuoso Space-Based Router can increase device routing productivity and reduce turnaround time by 50%.

Virtuoso floorplanner
A full custom and mixed-signal floor-planning set of tools, the Virtuoso floorplanner contains automatic and interactive floorplanning features to help designers develop layout from a schematic in a methodical manner. The floorplanner supports I/O constraint files, soft and hard rectilinear blocks, and layout and abstract views. Its features include a new pin-optimization engine with support for new pin group and guide (PGG) constraints, and the ability to configure and generate physical hierarchy. The floorplanner is unique in its ability to add value in both top-down and bottom-up methodologies.

ModGens
Module generators (ModGens) are designed to provide layout designers an intuitive way to quickly generate SKILL PCell instances into a complex, highly matched, and structured array. Within the ModGen tool, users specify the devices to be arrayed, then specify an interdigitating pattern, including insert dummy devices, body contacts, and guard rings.

ModGens can be created from either the schematic or the layout, using either a custom automatic generator for a high level of automation or by using the new placement pattern editor and topology routing objects for an interactive use model.
Virtuoso custom digital placer

The Virtuoso custom-digital placer automatically places standard-cell-based designs using more traditional row-based methods. This placer coupled with the Virtuoso Space-Based Router can be used to rapidly implement custom digital blocks within the Virtuoso environment.

Analog Auto-Placer

The Virtuoso Analog Placer is capable of a number of analog/RF-centric automatic placement functions. These functions include the automatic creation of quick placements and more robust placements that support more packing, as well as functions to fix DRC errors in the placement and to adjust cell pins and sides. The Virtuoso Analog Placer offers three modes of operation:

• Quick placement mode, which provides fast, DRC-aware placement for quick area estimation
• Quick placement as schematic mode, which provides placement-based device ordering in the schematic
• Fully automated placement with user-definable effort levels

Design migration

Virtuoso Layout Migrate enables fast migration of a given design to a new or altered process geometry. Integrated with the Virtuoso platform, it provides hierarchical, two-dimensional optimization algorithms to achieve significantly higher quality of results (QoR) than traditional methods using near-linear shrinks.

Interactive DRC fixing

Interactive DRC fixing is used for strategically fixing DRC errors in the layout in an automated fashion. This out-of-the-box technology runs natively on a Virtuoso OpenAccess technology file. The patented technology incrementally loads portions of the layout so that it can handle very large designs.

Specifications

Third-party support

• OpenAccess-compatible tools and functions
• PDKs (please contact your foundry provider for more information)

Design input

• OpenAccess database
• SKILL
• STREAM format
• OASIS format

Design output

• OpenAccess database
• SKILL
• STREAM format
• OASIS format

Platform/OS

• IBM AIX
• Linux

Cadence Services and Support

• Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
• Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
• More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
• Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

For more information, please visit www.cadence.com/support-and-training