cādence®

Virtuoso Variation Option
Advanced statistical exploration of your design

The Cadence® Virtuoso® Variation Option extends the statistical variation capabilities of the Virtuoso ADE Assembler and Virtuoso ADE Verifier to allow for more sophisticated analyses, and is especially well suited for advanced-node designs and designs requiring high-sigma validation.

Introduction to Virtuoso ADE Product Suite

The new Virtuoso ADE product suite enables designers to fully explore, analyze, and verify a design against design goals so that they can maintain design intent throughout the design cycle. As the industry's leading solution for analog simulation control and management, the Virtuoso ADE product suite allows users to flexibly select the product(s) that best support their design goals as they move through the design flow. The Virtuoso ADE Explorer provides a quick entry into the analysis process with easy execution of simulations, including support for running Monte Carlo statistics, corner sweeps, pass/fail analysis, and real-time tuning with the Virtuoso Spectre® Circuit Simulator.

The Virtuoso ADE Assembler extends the Virtuoso ADE Explorer's capabilities across multiple testbenches simultaneously, allowing the user to monitor all aspects of the larger analog block they are creating by enabling easy and direct review of all results and generating specification-comparison sheets and datasheets as needed. The Virtuoso ADE Assembler also contains targeted features for parasitic analysis, design migration

Virtuoso® ADE Suite

Virtuoso ADE Explorer

Virtuoso ADE Assembler

Virtuoso Variation Option

Virtuoso ADE Verifier

COMMON DATA EXCHANGE

Figure 1: Virtuoso ADE Product Suite

with parameter re-centering, and worst-case corner development to simplify variation analysis tasks. To handle the key challenges of advanced-node or high-sigma designs, the Virtuoso Variation Option enables fast Monte Carlo analysis for FinFETs, high-yield estimation, and yield-improvement flows. Finally, the Virtuoso ADE Assembler and Virtuoso ADE Explorer supply information to

the Virtuoso ADE Verifier, which is designed to match the highest level circuit specifications with individual analysis tests being developed by different users or design sites. Because status is managed in one location, as shown in Figure 1, circuit architects know the complete status of the design at all times.
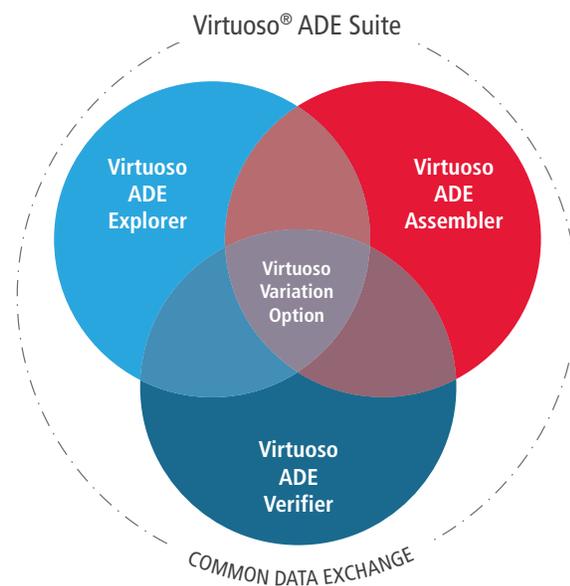
Virtuoso Variation Option Overview

The Virtuoso Variation Option supports extensive statistical exploration of your analog or RF design or custom digital design. Designed to work with the tests and specifications set up inside the Virtuoso ADE Explorer and Virtuoso ADE Assembler, it extends the native statistical capabilities of the tool into areas where more advanced analyses are required.

Benefits

- Enable the appropriate analysis by simply choosing your task (e.g., yield verification) or statistical corner creation and specify your target sigma requirement

- Efficient 3-sigma corner creation and yield verification with additional speed-up for FinFETs

- Provides high-yield estimation capabilities for checking the outer boundaries of your design at the 4-, 5-, or 6-sigma level

- Mismatch contribution analysis and statistical sensitivity analysis to pinpoint most influential devices within a statistical simulation

- Integrated yield improvement flow runs a series of analyses to tighten your yield factor to the highest number possible

- Close integration with the Virtuoso Schematic Editor and Virtuoso Layout Suite for fast test development and debug of physical effects introduced into the design during layout

Features

Task-driven user interface

Designing for yield traditionally involves repeatedly tuning your design and running Monte Carlo simulations. This method is very time-consuming and can easily lead to under-design or over-design if the number of Monte Carlo samples is not specified correctly. A much more efficient flow is to first create statistical corners that represent your circuit's worst-case conditions, then design against these

65nm   32nm   16nm

Smaller size
Larger variation

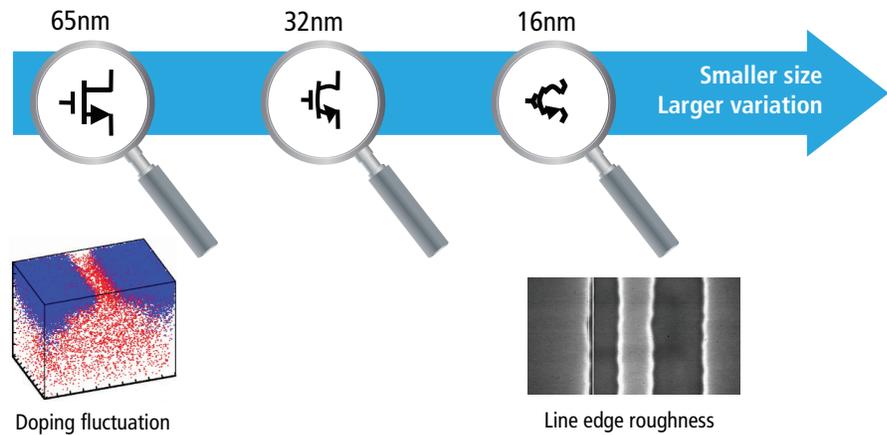Doping fluctuation   Line edge roughness

Figure 2: Variation challenges increase at 16nm and below

corners, and finally verify the yield. With the task-driven user interface, you only need to specify the task (verify the yield or create statistical corners) and your yield requirement, and the most appropriate algorithm that provides orders of magnitude speedup against traditional methods will be automatically set up.

Efficient 3-sigma analysis

The widespread adoption of FinFET technology at 16nm and below presents a new set of challenges for variation analyses, as shown in Figure 2.

These challenges impose significant risk on the design specifications if they are not properly analyzed both before

and after the physical implementation. However, the number of statistical simulations required, coupled with the number of transistors typically present in this type of design, makes traditional brute-force methods to calculate statistical variance impractical. Two algorithms are provided for fast, accurate 3-sigma analysis.

The first algorithm creates 3-sigma corners quickly, requiring a maximum of only 200 Monte Carlo samples. For strongly linear outputs, only 50 points may be needed to fit the model (by comparison, brute-force Monte Carlo analysis generally requires 2,000 samples). Choose the fast statistical corner
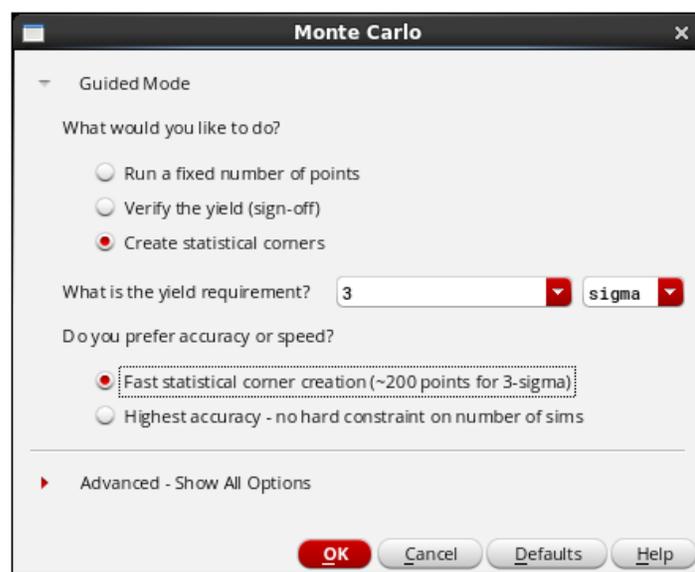

Figure 3: Create 3-sigma statistical corners

algorithm if you have a firm simulation budget, which creates corners as accurately as possible within the budget.

The second algorithm applies Monte Carlo reordering to speed the analysis process without accuracy loss. By working with leading foundries, this flow is even more efficient for FinFETs by calling foundry-provided APIs to speed up analysis, as shown in Figure 4. The sample reordering algorithm is available for both yield verification and creating corners.

High-yield estimation for 4-, 5-, or 6-sigma analysis

Parametric high-yield estimation is often required on devices that have extremely high volume (i.e., memory devices) or when testing the circuit limits is a must when failure of the part is not an option (i.e., automotive safety or medical devices). But a 6-sigma means testing to determine that the circuit failures are less than 2 parts-per-billion or 99.9999998%, rendering traditional Monte Carlo analysis completely impractical.

Two methods are provided to our users and are chosen depending on the conditions that the circuit is being tested under:

- Scaled-sigma sampling (SSS): This preferred statistical method generates samples where the standard deviation has been scaled up, which is more accurate than WCD for nonlinear behavior and more efficient when there is a large number of statistical parameters and specifications.

- Worst-case distance (WCD): This statistical method defines the shortest distance from the nominal point to the specification boundary in the process/mismatch parameter space. WCD typically requires under 100 simulations for each spec and so is suitable for designs with a small number of specs/parameters that need to be monitored/changed.

Mismatch contribution analysis

Mismatch contribution analysis is a Monte Carlo post-processing feature that helps in identifying the important contributors to mismatch variation. You can then modify the identified devices in the schematic (Figure 5) and make the design less
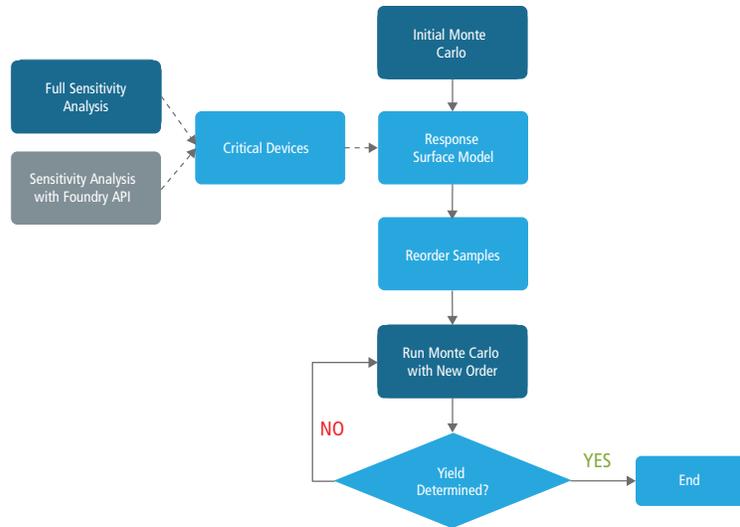

Figure 4: Cadence's new method for statistical analysis of FinFETs

sensitive to mismatch variation. You can apply this method to existing standard Monte Carlo results or use the Sensitivity Accuracy method to automatically run the minimum required number of points.

Specifications

Analyses

- Works seamlessly with Virtuoso ADE Assembler and Virtuoso ADE Explorer

- Support of matching and correlation constraints from Virtuoso Schematic Editor XL

- High-performance statistical analysis, with additional speedup for FinFETs

- Integration with Virtuoso Multi-Mode Simulation

- Creation of simulation corners from statistical analysis

Figure 5: Use mismatch analysis to identify the most critical devices in the design.

- Cross-probing and annotation to schematics and layout
- Automated yield improvement flow based on optimization and/or statistics
- High-sigma statistical corner development

Visualization

- Histograms showing pass/fail regions
- Scatter plots
- Quantile plots with normality test
- Plot/print value, yield, mean, sigma vs. sample iteration
- Correlation tables
- Built-in waveform calculator

Distributed processing

- Distribution of multiple simulations
- Efficient use of computer farms
- Built-in basic load balancing and interface to other load-balancing tools
- Job monitoring and controlling functions
- GUIs for set-up and viewing status

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/support-and-training