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Virtuoso Variation-Aware Implementation Option

Fast path to determining physical implementation impact on your design

Physical implementation has a substantial impact on whether your design will meet its specifications. With the partial layout resimulation capability of Cadence® Virtuoso® Variation-Aware Implementation Option, you can test as you proceed through your design process. The capability mixes schematic and layout representations in the same netlist, to help you refine your design faster.

Virtuoso Variation-Aware Implementation Option

Virtuoso Variation-Aware Implementation Option provides you with a fast path to determining how the physical implementation impacts your design. Its partial layout resimulation capability lets you:

- Check that your assumptions about critical paths in your design are correct
- Complete a layout of a critical block early on
- Analyze partial placement and partial routing (using the Cadence Virtuoso Layout Suite for Electrically Aware Design license)

Integration with Virtuoso Platform

Virtuoso Variation-Aware Implementation Option stitches together the device parameters extracted from a partial layout with the schematic devices for a missing layout. The resulting single netlist can be resimulated inside Cadence Virtuoso Analog Design Environment. The license for the option supports both a MODGEN constraint flow and a real layout flow. While the partial layout resimulation flow doesn't replace signoff, it can eliminate unnecessary design iterations and over-design.

If you use Cadence Virtuoso Integrated Physical Verification System (IPVS), you can use the device parameter extraction in the product to calculate the quantities needed to move from the physical representation to the electrical representation for resimulation.

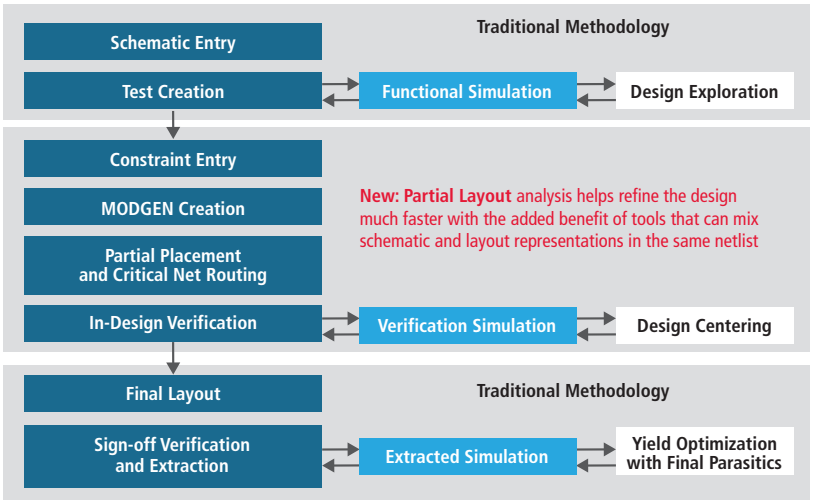

Figure 1: Variability-aware design

Managing Layout-Dependent Effects

Layout-dependent effects (LDEs) are introducing a new level of variability to planar transistor designs between 65nm and 20nm, impacting device performance and characteristics. That's why it's important to account for LDEs at the earliest stages of your design. Virtuoso Variation-Aware Implementation Option performs partial layout simulation. Doing so, the

tool provides a shortcut to determining the impact of physical implementation on your design.

Circuit design advantages of Virtuoso tool

In a traditional circuit design flow, physical effects can sometimes be modeled by making assumptions. But the "true" parasitics are typically not discovered until a full layout has been created and sent through a time-consuming serialized methodology for validation and extraction. Consequently, parasitic issues are detected very late in the design process, when they can be difficult to correct easily.

At advanced nodes, physical effects become increasingly important. LDEs—from well proximity effects to poly spacing effects, length of diffusion, and oxide definition (OD) to OD spacing effects—can change transistor characteristics anywhere from 20 percent up to 80 percent. Furthermore, these effects could result in longer turnaround times and electrical performance degradation.

Pre-layout simulation, even with their assumptions about device characteristics, are no longer accurate enough at these nodes to be effective. However, through the partial layout simulation capabilities of the Virtuoso Variation-Aware Implementation Option, you can:

Layout-Dependent Effects		Prior to 40nm	At 40nm	28nm and Beyond
WPE	**Well Proximity Effect**	•	•	•
PSE	**Poly Spacing Effect**		•	•
LOD	**Length of Diffusion**	•	•	•
OSE	**OD to OD Spacing Effect**		•	•

Table 1: Impact of LDEs at advanced nodes

- Choose a user-configurable combination of Pcells, MODGENs, and auto-placement to quickly generate prototype layouts (partial or complete) to resimulate with accurate layout effects and debug problems
- Use in-design verification to detect trouble areas during detailed layout generation and to verify constraints specified by the circuit designer for electrical matching
- Use signoff layout versus schematic (LVS) and extraction flows for final verification of circuit behavior with both layout effects and interconnect parasitics

Layout design advantages of Virtuoso tool

For layout designers following the traditional flow, circuits are designed to meet specifications based on device sizes and process variation. Circuits are verified using corners and Monte Carlo analysis, prior to being handed off for layout. LDEs usually aren't considered. Yet, transistor device characteristics do vary depending on context, placement, and density of neighboring transistors.

With Virtuoso Variation-Aware Implementation Option as part of your flow, you can:

- Detect and easily fix LDE variability hotspots early through integration with the Cadence Litho Electrical Analyzer inside Cadence Virtuoso DFM
- Benefit from real-time LDE estimation with post-simulation accuracy
- Minimize discrepancies between layout and schematic-extracted simulations

Foundry-specific calculators can also be used as part of this flow. Contact your particular foundry provider for additional information.

More Information

For more details about electrically aware design, read the Virtuoso Layout Suite for Electrically Aware Design datasheet and watch the archived TSMC and Cadence webinars on addressing LDEs in advanced-node design.

Cadence can also bring to your company an LDE workshop. Contact your local Cadence sales office for more details.

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