Cadence Virtuoso Layout Suite for Electrically Aware Design
Enhancing design team productivity and circuit performance for custom ICs

By enabling you to monitor electrical issues while you create your layout, Cadence® Virtuoso® Layout Suite for Electrically Aware Design (EAD) enhances design team productivity and circuit performance for custom ICs. The solution provides the technology and methodology to enable you to avoid multiple design iterations and “over design” and save days to weeks of design time. With enhanced real-time visibility into electrical issues, layout and circuit designers can collaborate more efficiently.

Virtuoso Layout Suite EAD works seamlessly with other tools in the Virtuoso platform. As a result, you can capture currents and voltages from simulations run in Virtuoso Analog Design Environment and pass this electrical information into the layout environment.

Save Weeks to Days of Design Time
With its unique in-design electrical verification capability, Cadence Virtuoso Layout Suite for Electrically Aware Design (EAD) enhances design team productivity and circuit performance for custom ICs. The solution provides the technology and methodology to enable you to avoid multiple design iterations and “over design” and save days to weeks of design time. With enhanced real-time visibility into electrical issues, layout and circuit designers can collaborate more efficiently.

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Key Benefits
- Reduces circuit design cycle by up to 30 percent
- Enables you to enhance chip performance and utilize less area
- Minimizes respins and “over design”

Key Features
- Built-in interconnect parasitic extraction engine
- Random walk field solver option for high-precision extraction
- Electrical constraint management
- Interactive signal electromigration analysis
- Interactive point-to-point interconnect analysis
- Partial layout resimulation, with no need for layout versus schematic (LVS) to get extraction results

Figure 1: With an electrically aware design flow, you can identify and resolve electrical issues early in your design cycle

- Strengthens layout and circuit design collaboration
Parasitic extraction engine

Virtuoso Layout Suite EAD features a built-in interconnect parasitic extraction engine that lets you perform real-time analysis and optimization. The engine, which also works on partial designs, extracts parasitics in real time and stores them in a Cadence OpenAccess® database. The parasitics are displayed in informational “balloons” that appear on the GUI, making it easy for you to quickly evaluate your layout as it is created—and address any issues before it is too late in the design cycle.

The tool’s parasitic extraction suite provides solutions to meet the diverse needs of analog and custom design teams. Its fast extraction provides parasitic data on-the-fly as your layout is being created or modified. For critical paths where the highest extraction accuracy is required, the solution’s optional, built-in random walk solver is available; users can control the accuracy versus performance trade-offs directly on a global or net-by-net basis.

Virtuoso Layout Suite EAD provides a multi-resolution extraction option where you can easily select nets to be solved at high accuracy, critical nets to be solved at the highest accuracy, and others with fast extraction. The extraction and solver solutions are fully multi-threaded so that performance can be tailored and maximized for available computational resources. Figure 2 shows the solution’s parasitic extraction engine in action.

Electrical constraint management

The solution’s electrical constraint management function provides you with a means to set electrical constraints and then observe, in real time, whether these constraints are being met.

Signal electromigration analysis

The solution’s interactive signal electromigration (EM) analysis function highlights EM violations on layout using a color map. You can cross-probe between the EM browser and your layout to quickly spot—and fix—problem areas. The tool does provide hints to recommended widths for given wire segments to meet EM requirements. The interactive point-to-point analysis tool lets you easily identify, between any two points on the same net:

- EM violations
- Path resistance
- Limiting resistance

Partial layout resimulation

In the traditional flow, a series of layout decisions are made with little awareness of the electrical impact. Devices, cells, and blocks are placed and routed by the layout designer, but these decisions are made based on previous best practices, not on how these decisions will actually impact electrical performance. Because an LVS clean layout is a pre-requisite to running parasitic extraction (Rs and Cs on nets), it has been impossible to understand the impact of layout decisions until late in the design process. This can lead to multiple iterations to reach design closure, or, alternatively, design teams over-design, basically sacrificing performance to meet the increasingly complex reliability and EM requirements. The costs of not having electrically aware layout are longer time to market, increased die area, and lower circuit performance. Advanced nodes exacerbate these costs.

Virtuoso Layout Suite EAD changes the design paradigm. Used together with Virtuoso Analog Design Environment XL, Virtuoso Layout Suite EAD lets you resimulate designs with parasitics from partial layout in the Virtuoso Analog Design Environment XL. You can incrementally design the circuit and layout to meet specifications with layout effects.

Learn More

Virtuoso Layout Suite EAD is available now. For more information, visit http://www.cadence.com/products/cic/electrically_aware_design/pages/default.aspx.