

Virtuoso Analog Design Environment GXL

Variation analysis simplified

Cadence® Virtuoso® Analog Design Environment GXL provides all the capabilities of Virtuoso Analog Design Environment L and XL for thorough exploration and validation of a design. Additionally, Virtuoso Analog Design Environment GXL enables you to explore parasitic effects and sensitivities to improve yield; create design-specific worst-case corners; and find the optimum design over nominal, corner, or target yield. A flexible licensing methodology further ensures a cost-effective application of the tool's capabilities.

Maintain Design Intent Through Your Design Cycle

The Virtuoso Analog Design Environment product suite provides all the capabilities required to fully explore, analyze, and verify a design against your desired goals, allowing you to maintain design intent throughout the design cycle. As the industry's leading solution for analog simulation control and management, it allows you to flexibly select the tier that best supports your design goals as they move through the design flow. Virtuoso Analog Design Environment L provides a quick entry into the analysis process with easy execution of simulations. Virtuoso Analog Design Environment XL extends the L tier capabilities, providing multiple test support, analysis over sweeps, corners, and Monte Carlo simulations; supporting easy review of all results directly; and generating spec-comparison sheets and datasheets as needed. Virtuoso Analog Design Environment GXL builds on L and XL capabilities by providing targeted tools that aid with key design challenges with early parasitic analysis, design centering, and designing in multi-technologies.

Virtuoso Analog Design Environment GXL Overview

Virtuoso Analog Design Environment GXL uses the same advanced design and simulation cockpit as Virtuoso Analog Design Environment XL, and includes extended analysis capabilities for more detailed design exploration. A user can choose to launch Virtuoso Analog Design Environment GXL directly or just access the additional analysis capabilities from Virtuoso Analog Design Environment XL.

Benefits

- Features extensive design exploration with sensitivity and mismatch variation contribution analyses
- Manual tuning and advanced optimization algorithms improve design centering within multiple specifications
- Built-in parasitic estimation flow helps design convergence by making it possible to quickly identify and analyze parasitic sensitivities prior to layout

- Support for multiple technologies facilitates multi-power domain design analysis
- Generates worst-case corners for your design, including deriving specific corner cases from statistical simulation data
- Schematic migration tool plus optimization helps you quickly retarget your design from one process to another
- High-yield estimation tool provides you with accurate estimations of four, five, or six-sigma distributions for your circuits

Features

Extensive design exploration

To further understand the behavior of a design, you can run sensitivity analysis to identify weaknesses in a design to process variations and for design sizing. You can then automatically create design-specific corners for signoff-level simulation.

Built upon the statistical analysis capabilities in Virtuoso Analog Design Environment XL, the tool provides mismatch analysis capabilities that

you can use to further explore the sensitivities of a design for all or a selected set of devices.

For designs where a high-yield margin is critical, such as memory, a high-yield analysis capability provides up to six-sigma accuracy, without the cost of running extensive Monte Carlo simulations.

Parasitic resimulation

Explore parasitic effects early in the design flow with the ability to assign parasitic estimates onto nets and ports of your design, without editing the schematic. An estimated view is compiled for simulation across all the tests and analysis options available in Virtuoso Analog Design Environment XL or GXL to identify areas to focus on in the design development. Similarly, post-layout extracted designs can also be submitted for validation against the design goals or compared against the original parasitic estimates. Parasitic effects can be easily copied from an extracted view back to an estimated view to gain full access to all the debug capabilities in Virtuoso Analog Design Environment GXL.

Design centering

With the set-up of tests and specifications already available in Virtuoso Analog Design Environment XL, you can simply add the range of devices you want to explore and use Virtuoso Analog Design Environment GXL optimization engines to find the optimum design. The tool includes an array of local and global optimization choices, so you can control how the optimizer runs to center a design over nominal, defined corners and with parasitic estimates in place. Manual tuning techniques are also provided to give you maximum control over the optimization choices and limits.

Design for yield

Use a series of optimization methods, along with your corners process files, to center your design values and maximize yield in a more automated way. For circuits requiring high design margins

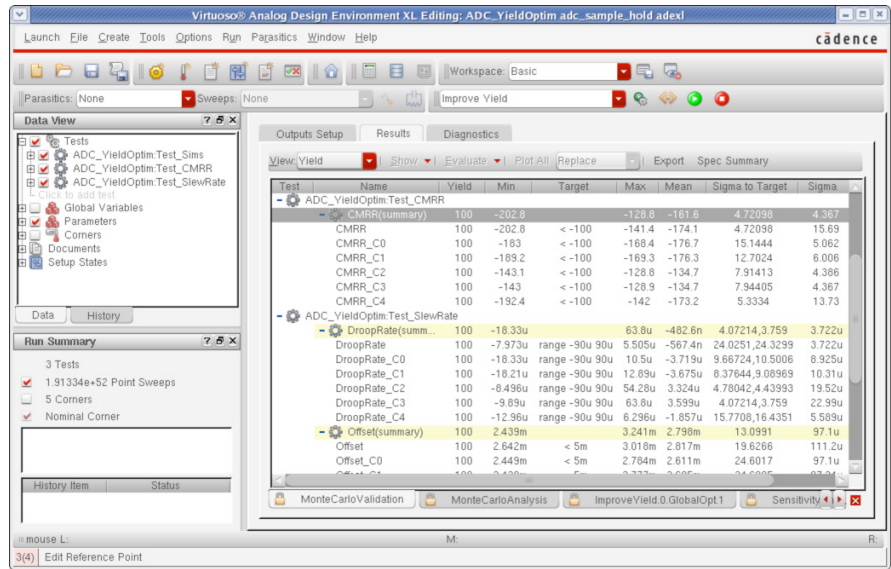


Figure 1: Virtuoso Analog Design Environment GXL: Extends analysis into parasitics and yield

up to six-sigma, the internal design goals are tightened as it optimizes the parametric yield.

Multi-technology support

Technology support is available to aid in the design of complex multi-chip solutions and/or multiple power domains within the same circuit, and integrate them into a single package in conjunction with the Cadence Allegro® system interconnect design platform.

Specifications

Extended analyses

- Inherits all features and functionality from Virtuoso Analog Design Environment XL
- Sensitivity analysis on design parameters, statistical parameters, and design variables

Mismatch analyses

- Ability to generate design-specific corners
- High-yield measurement

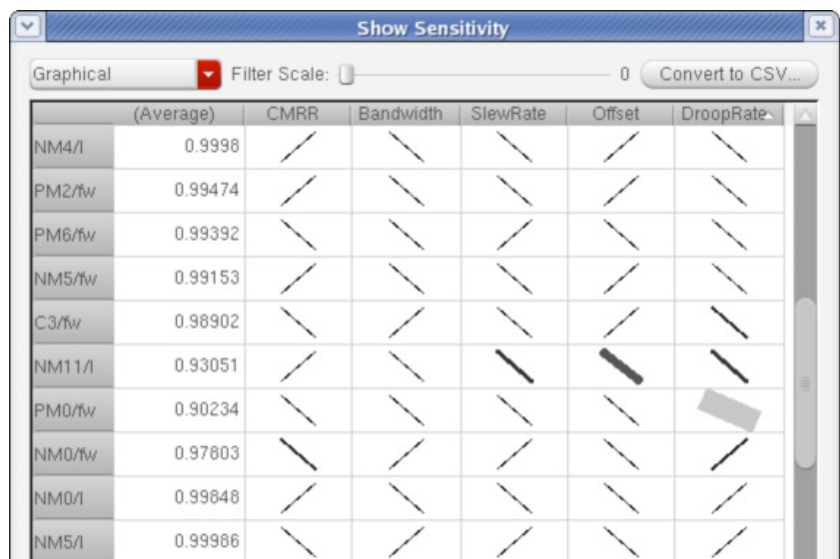


Figure 2: Sensitivity of device parameters to measured goals

- Multiple technology support with Allegro platform to enable System-in-package (SiP) design

Parasitic analysis

- Supports exploration of design parasitic effects before layout
- Adds R, L, C, or K parasitic elements without altering the schematic
- Full simulation support of post-extracted layouts
- Compare pre- and post-layout parasitic effects

Optimization options

- Take advantage of four local and global algorithm choices
- Optimize nominally or over corners, with or without parasitic estimates
- Run optimization with or without a starting point
- Use for retargeting designs to new processes
- Improves design yield and design centering up to six-sigma margins

Design inputs

- OpenAccess data objects
- Cadence proprietary languages: OCEAN and Spectre® MDL
- SPICE netlists
- Circuit design language (CDL)
- VHDL IEEE 1076-1993
- Verilog® IEEE1364
- PSF and PSF XL waveform formats
- SST2 waveform format
- Cadence SKILL

Design outputs

- XML database
- PSF and PSF XL
- SST2
- Comma Separate Value
- Cadence proprietary script language: OCEAN

Platform/OS

- X86 Linux
- Sun Solaris
- IBM AIX

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



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