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Virtuoso ADE Verifier

Analog specification verification cockpit

Cadence® Virtuoso® ADE Verifier is designed to provide the analog verification engineer or architect a global view of the circuit status. Part of the Virtuoso ADE product suite, the Virtuoso ADE Verifier works in conjunction with Virtuoso ADE Assembler and Virtuoso ADE Explorer, enabling tests created in those environments to be linked to the highest level design requirements and monitored to ensure all aspects of the design are coming together as planned. Together, these tools provide a cohesive and complete design solution for analog, custom, RF, and mixed-signal ICs.

Introduction to Virtuoso ADE Product Suite

The new Virtuoso ADE product suite enables designers to fully explore, analyze, and verify a design against design goals so that they can maintain design intent throughout the design cycle. As the industry's leading solution for analog simulation control and management, the Virtuoso ADE product suite allows users to flexibly select the product(s) that best support their design goals as they move through the design flow. The Virtuoso ADE Explorer provides a quick entry into the analysis process with easy execution of simulations, including support for running Monte Carlo statistics, corner sweeps, pass/fail analysis, and real-time tuning with the Virtuoso Spectre® Circuit Simulator.

The Virtuoso ADE Assembler extends the Virtuoso ADE Explorer's capabilities across multiple testbenches simultaneously, allowing the user to monitor all aspects of the larger analog block they are creating by enabling easy and direct review of all results and generating specification-comparison sheets and datasheets as needed. The Virtuoso ADE Assembler also contains targeted features for parasitic analysis, design migration with parameter re-centering, and worst-case corner development to simplify variation analysis tasks. To handle the key challenges of advanced-node or high-sigma designs, the Virtuoso Variation Option enables fast Monte Carlo analysis for FinFETs, high-yield estimation, and yield-improvement flows. Finally, the Virtuoso ADE Assembler and Virtuoso ADE Explorer supply information to the Virtuoso ADE Verifier, which is designed to match the highest level circuit specifications with individual analysis tests being developed by different users or design sites. Because status is managed in one location, as shown in Figure 1, circuit architects know the complete status of the design at all times.

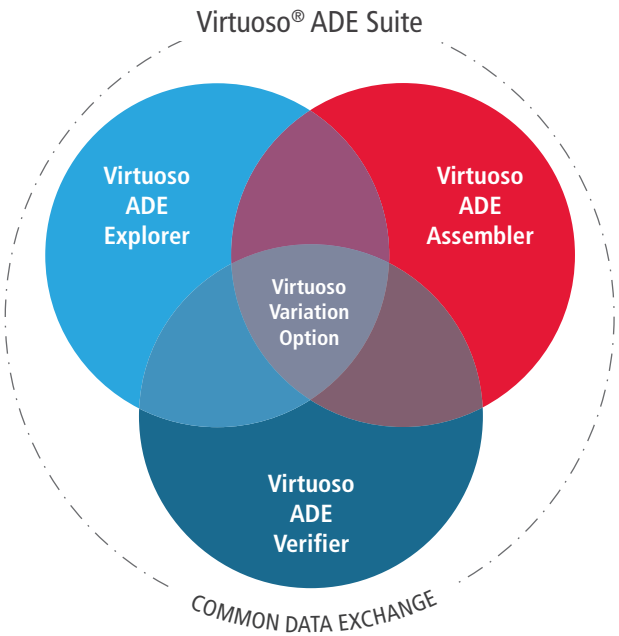

Figure 1: Virtuoso ADE Product Suite

Virtuoso ADE Verifier Overview

Virtuoso ADE Verifier enables analog electrical design verification, which is a new concept to many analog design engineers. It provides high-level overview of an entire design, linking high-level requirements such as power consumption, gain, and bandwidth to the individual tests that are being created for specification measurement. Virtuoso ADE Verifier can link together a group of specification measurement tests across multiple designers or locations and provide the pass/fail status in one easy-to-read window. The Virtuoso ADE Verifier can also quickly identify requirements that have no assigned measurements, and offer visual clues if too few tests are linked to a particular measurement.

Users can choose to first enter the high-level specifications and blocks that will be tested, parceling out the specific test creation and simulations to individual engineers. Or, if the tasks have already been assigned through a traditional method, the Virtuoso ADE Verifier can load in the tests and any results achieved in the Virtuoso ADE Explorer or Virtuoso ADE Assembler and link them to the high-level specifications. Once the connections are in place, updates are easily managed because the Virtuoso ADE Verifier is integrated into the Virtuoso platform. Regression runs can be triggered for late changes, across a single group of tests or all of them. See Figures 2 and 3.

Benefits

- Links together high-level design requirements with the individual tests to guarantee requirements are being met
- Linked tests can come from multiple engineers and/or design sites
- Integration into the Virtuoso custom design platform helps identify changes occurring in leaf tests so tests are kept in sync
- New simplified scripting language makes it easy to create command line regression scripts
- Extensive job monitoring allows verification engineer to monitor failures during simulation execution

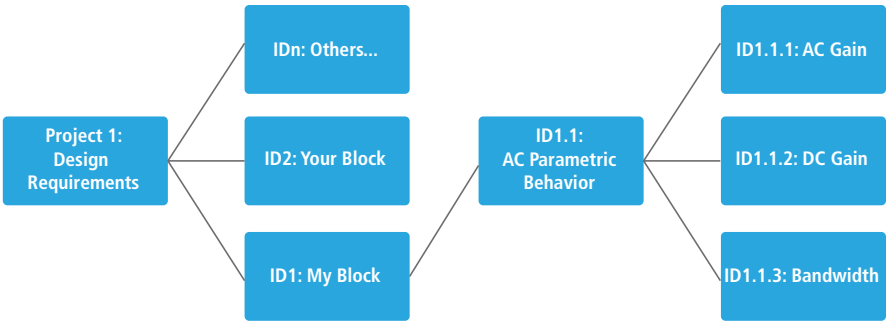

Figure 2: Example verification structure

- Does not require write permission to the tests individual engineers have created
- Can run any analysis from Virtuoso ADE Explorer or Virtuoso ADE Assembler to complete the regression
- Configurable run sequencing to allow one set of results to be used in the next set of runs
- Failures easily detected and traced to specific tests

Features

Planning flow for analog design

Virtuoso ADE Verifier is designed to allow the entry of high-level design specifications that must be achieved by all the blocks in the design. Specific blocks can be identified, and proposed tests created then documented to specify what needs to occur in the block design. This planning flow allows the chip architect to begin by identifying the chip "needs" first, parceling them out across the design teams to set up specific tests that measure various specifications. Once the engineers create the specific tests, which can include any capability inside the Virtuoso ADE Explorer or Virtuoso ADE Assembler, the tests are linked back to the high-level specification. Simulation information is also linked back so that overall design goals can be viewed and the pass/fail/run status immediately seen. The Virtuoso ADE Verifier is designed to handle significant supporting documentation that can be used to fully document the blocks, including which tests were created and why, status of simulation runs, dates, engineers, and design location. See Figure 4.

Integration flow for analog design

Virtuoso ADE Verifier can also be used to create the high-level specification hierarchy after individual tests have already been created. This feature is useful when the design is divided among individual engineers outside of the Virtuoso platform. Bringing all the parts back together in a fully integrated cockpit makes it easy to see if tests are out-of-

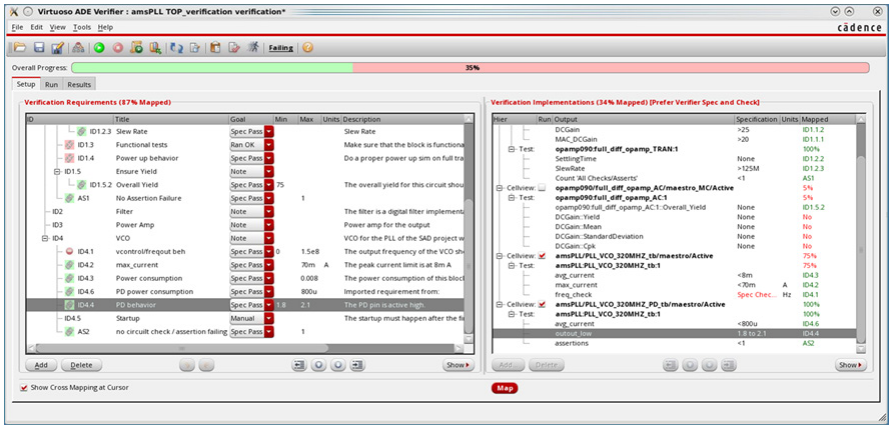

Figure 3: Virtuoso ADE Verifier cockpit

date, or if particular specifications have been missed or are in conflict in different parts of the design. In addition, pulling all the tests back together in a single location enables any late changes to be run by the Virtuoso ADE Verifier to see if any tests start failing. Engineers affected by failures can be notified that the change has impacted their portion of the design.

Job monitoring

Simulation jobs can be monitored whether they are run from within the GUI or use command-line scripting. The job monitor window shows test progress, and can inform the architect about any failures within the run that need further investigation. Runs can be launched, sorted, and stopped from this single window. See Figure 5.

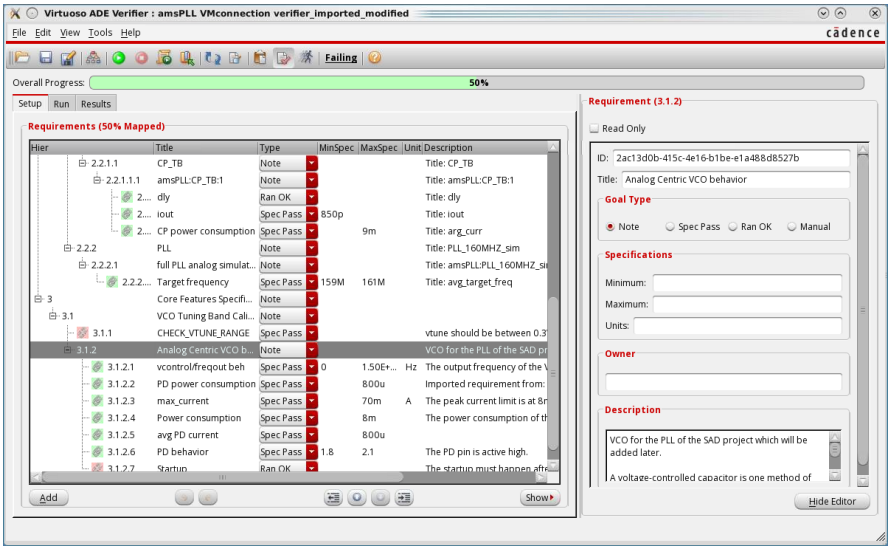

Figure 4: Virtuoso ADE Verifier planning flow example

Specifications

Interactive verification control

- Link high-level requirements to base test configurations
- Easily determine status of leaf tests (pass/fail/run/not run)
- Job monitoring for verification tests run within the tool or through scripts on the command line
- Integrates with Spectre Circuit Simulation platform
- Easily see whether you have enough test coverage for all of your design requirements over a variety of circuit conditions
- Create verification reports in test, HTML, or XML for design reviews
- API code allows for customization
- Designed to work well with Virtuoso ADE Explorer and Virtuoso ADE Assembler, sharing a common database view so data flows easily from one tool to the next and back again

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
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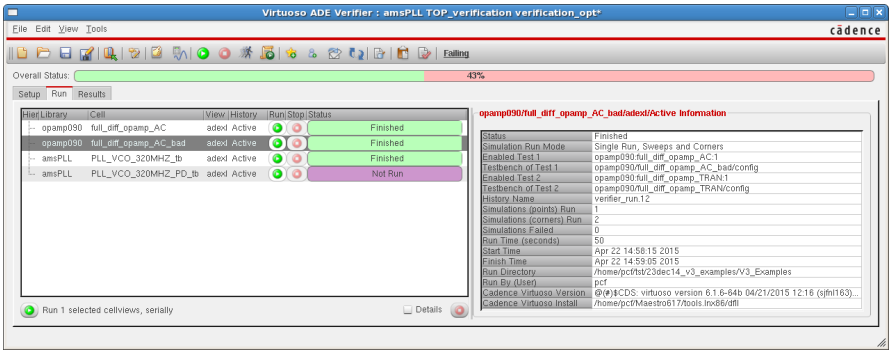

Figure 5: Virtuoso ADE Verifier job monitor

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