

## Virtuoso ADE Assembler

Extensive design exploration, simulation, and verification

Cadence® Virtuoso® ADE Assembler is an advanced design and simulation environment that extends the capabilities of Virtuoso ADE Explorer, adding all the tests needed to fully verify a design over all operational, process, and environmental conditions. As more analysis is required, users can take incremental advantage of the Virtuoso Variation Option to do more advanced statistical analysis on their design. Part of the Virtuoso ADE product suite, Virtuoso ADE Assembler is designed to work independently and with the Virtuoso ADE Explorer and Virtuoso ADE Verifier to provide a cohesive and complete design solution for analog, custom, RF, and mixed-signal ICs.

### Introduction to Virtuoso ADE Product Suite

The new Virtuoso ADE product suite enables designers to fully explore, analyze, and verify a design against design goals so that they can maintain design intent throughout the design cycle. As the industry's leading solution for analog simulation control and management, the Virtuoso ADE product suite allows users to flexibly select the product(s) that best support their design goals as they move through the design flow. The Virtuoso ADE Explorer provides a quick entry into the analysis process with easy execution of simulations, including support for running Monte Carlo statistics, corner sweeps, pass/fail analysis, and real-time tuning with the Virtuoso Spectre® Circuit Simulator.

The Virtuoso ADE Assembler extends the Virtuoso ADE Explorer's capabilities across multiple testbenches simultaneously, allowing the user to monitor all aspects of the larger analog block they are creating by enabling easy and direct review of all results and generating specification-comparison sheets and datasheets as needed. The Virtuoso ADE Assembler

also contains targeted features for parasitic analysis, design migration with parameter re-centering, and worst-case corner development to simplify variation analysis tasks. To handle the key challenges of advanced-node or high-sigma designs, the Virtuoso Variation Option enables fast Monte Carlo analysis for FinFETs, high-yield estimation, and

yield-improvement flows. Finally, the Virtuoso ADE Assembler and Virtuoso ADE Explorer supply information to the Virtuoso ADE Verifier, which is designed to match the highest level circuit specifications with individual analysis tests being developed by different users or design sites. Because status is managed in one location,

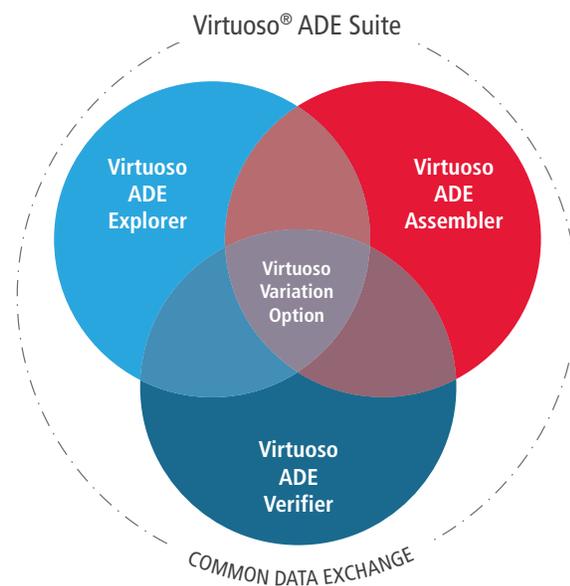


Figure 1: Virtuoso ADE Product Suite

as shown in Figure 1, circuit architects know the complete status of the design at all times.

## Virtuoso ADE Assembler Overview

Virtuoso ADE Assembler—the advanced design and simulation environment for the Virtuoso platform—supports extensive exploration of multiple designs against their objective specifications, setting the standard in thorough, fast, and accurate design and variation analysis and verification capabilities. It works seamlessly with Virtuoso ADE Explorer, which is included with the Virtuoso ADE Assembler license. The Virtuoso ADE Assembler enables the user to netlist and simulate partial layouts to allow detailed analysis of layout-dependent effects, and when used with the Virtuoso Variation Option, analyze advanced node variation, high-yield estimation and statistical sensitivity. See Figure 2.

### Benefits

- Built-in “run plans” simplify the creation and execution of small sets of regression tests, both interactively and with a new regression scripting language
- Design analysis across multiple tests and conditions simultaneously enables thorough design validation and compiles results into a single easy-to-use database
- Support for corners, parametric sweeps, Monte Carlo, and reliability analysis across multiple tests
- Built-in advanced variation analysis tools, such as worst-case corners and statistically derived corners
- Quick color-coded feedback of all results against target specifications to help maintain design intent
- Optimum analysis throughput with simulation distribution and multi-test management across user-preferred load balancing software

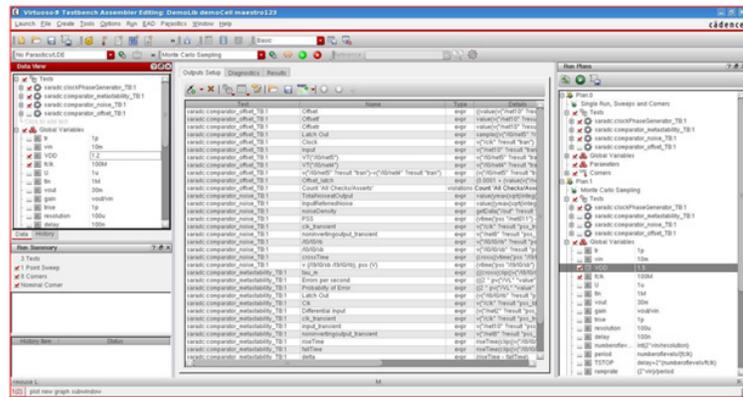


Figure 2: Virtuoso ADE Assembler cockpit showing run plans

- Simplification of design reviews through integral documentation, specifications, measurement results, and waveforms
- Substantial performance enhancements throughout, especially for test database versioning and waveform plotting
- Close integration with Cadence Virtuoso Schematic Editor and Virtuoso Layout Suite for fast test development and debug of physical effects introduced into the design during layout
- Full suite of parasitic analysis capabilities built-in

### Features

#### Specification-driven design

To accelerate design verification, Virtuoso ADE Assembler combines specification entry and design management in a single unified cockpit. A specification consists of all required tests, analyses, and operating conditions for validation against a measured set of goals. With Virtuoso ADE Assembler, you can easily develop multiple tests, along with all the different conditions to validate a design’s performance against the target specification. Each Virtuoso ADE Assembler session can be treated as a project, providing access to all the tests, sweeps, corners, scripts, and documentation needed to completely validate a design against the designer’s intent.

An overview of all the tests, simulators used, and analysis conducted—along with any defined variables and corners—is listed on the Data View assistant screen. Results of the latest analysis appear in a tabular view on the right side, with color coding to show at a glance the simulation results that pass or fail against the target specification. Results can be reordered or transposed for better visualization. Filters at the top of the datasheet allow quick manipulation of large lists to hone in on specific problem areas of the circuit. Users can easily explore results in more detail by right-clicking any single result or set of results that pops up in the Virtuoso Visualization and Analysis waveform window. In addition, a results history is automatically maintained so users can quickly go back to see previous results or even results from different test configurations. The new “run plans” can be used to quickly set up multiple tests and run them on a “conditional” basis, allowing results from one set of tests to be used in the next set as starting points. See Figure 3.

#### Sophisticated variation design

The Virtuoso ADE Assembler supports sophisticated variation analysis with a number of different built-in tools. Worst-case corners can be used to reduce large corner sets to a handful of those that provide the most circuit stress. This handful of corners can then be used to quickly check new measurements or design changes without having to

run the complete set. Local and global optimization algorithms are used in the design centering modes when moving designs from one process node to the next to help you maintain circuit yield. Tuning mode can help you tune your design quickly even across multiple test benches and multiple conditions. The engineer is in control in this mode and can make tradeoffs on the fly depending on how the results are converging. When combined with the Virtuoso Variation Option, Virtuoso ADE Assembler can be extended to include features to statistically analyze advanced node circuits more quickly, develop accurate pictures of the design behavior within a 4- to 6-sigma design space, and use automated techniques to enhance overall yield.

### Integral part of the Virtuoso custom design platform

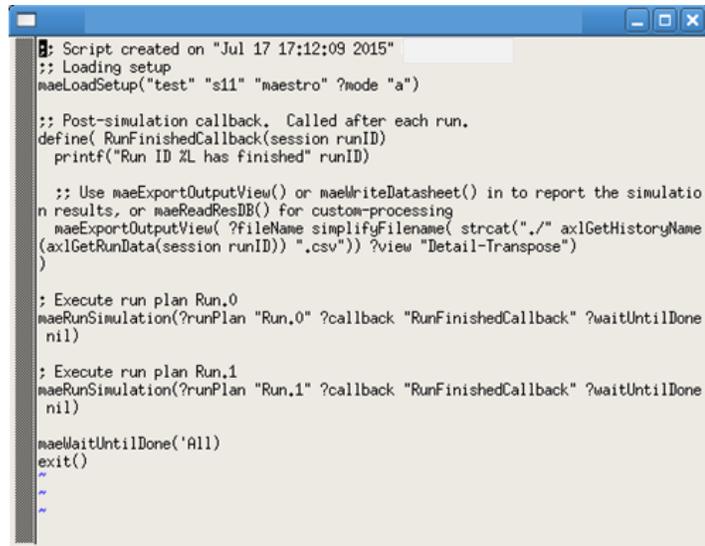
Virtuoso ADE Assembler is an integral part of the Virtuoso custom design platform. It bridges the gap between schematic design and physical layout by providing a simulation environment where the designer can compare designs in both pre- and post-extracted forms, thereby completing the Cadence IC design flow. It supports analog system to IC design methods with complete access to behavioral modeling languages for both simulation and cross-probing for waveform display. Post-simulation operating condition can be easily annotated back to the schematic with net voltages, currents, and device operating information.

When combined with the Virtuoso Implementation-Aware Design Option, Virtuoso ADE Assembler can be used as a central cockpit to analyze the layout as it is being created, giving the user the added benefit of seeing the effects of different layout choices early and providing guidance on how best to create layouts to negate the layout-dependent effects on the circuit.

## Specifications

### Interactive simulation control

- Works seamlessly with Virtuoso ADE Explorer for single test operation



```

Script created on "Jul 17 17:12:09 2015"
;; Loading setup
maeLoadSetup("test" "s11" "maestro" ?mode "a")

;; Post-simulation callback. Called after each run.
define( RunFinishedCallback(session runID)
  printf("Run ID %L has finished" runID)

  ;; Use maeExportOutputView() or maeWriteDatashet() in to report the simulation
  n results, or maeReadResDB() for custom-processing
  maeExportOutputView( ?fileName simplifyFilename( strcat("./" axlGetHistoryName
(axlGetRunData(session runID)) ".csv") ) ?view "Detail-Transpose"
)

; Execute run plan Run.0
maeRunSimulation(?runPlan "Run.0" ?callback "RunFinishedCallback" ?waitUntilDone
nil)

; Execute run plan Run.1
maeRunSimulation(?runPlan "Run.1" ?callback "RunFinishedCallback" ?waitUntilDone
nil)

maeWaitUntilDone('All)
exit()

```

Figure 3: Example "run plan" that is auto-generated for easy regression scripting.

- Design exploration with sweeps, corners, and Monte Carlo analysis across multiple test benches and conditions
- Global and local optimization modes
- Reliability analysis

- Support of matching and correlation constraints from Virtuoso Schematic Editor XL
- Creation and tracking of parametric dependencies among tests for more complex analysis
- Integrates with Spectre Circuit Simulation platform
- Ability to save different test configurations for different steps in the testing flow and analysis of results
- Creation of specifications directly from simulation results
- Quick overview window of test results against target specification
- Cross-probing and annotation to schematics and layout
- Support for pre-run calibration scripting

### Built-in variation analyses

- Worst-case corner analysis
- K-sigma statistical corner development
- Design migration and centering mode for moving between process nodes
- Cross test tuning to aid design centering

### Waveform display

- Supports multiple y-axes, strip plots, and Smith charts
- Built-in waveform calculator
- Independent sub-window displays
- Horizontal and vertical measurement markers
- Independent pan and zoom capability
- User-defined labels and titles
- Color and line style controls
- Signal browser
- Color-coordinated cross-probing to schematics

### Distributed processing

- Distribution of multiple simulations
- Efficient use of computer farms
- Built-in basic load balancing and interface to other load-balancing tools
- Job monitoring and controlling functions
- Graphical user interfaces for set-up and viewing status

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit [www.cadence.com/support-and-training](http://www.cadence.com/support-and-training)



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