

Spectre Accelerated Parallel Simulator (APS)

Advanced mixed-signal simulation solution

The Cadence® Spectre® Accelerated Parallel Simulator (APS) is an analog SPICE simulator that provides Spectre accuracy with a 5X reduction in simulation time compared to the classic Spectre Circuit Simulator. Spectre APS provides optimized performance for simulation of leading-edge analog and RF designs.

Spectre Simulation Platform

As the industry's leading solution for accurate analog simulation, the Spectre Simulation Platform contains multiple solvers to allow a designer to move easily and seamlessly between circuit-, block-, and system-level simulation tasks. The foundation of the platform is a unified set of technologies shared by all of the engines—the parser, device models, Verilog-A behavioral modeling, input data formats, output data formats, etc.—thereby guaranteeing consistent and accurate evaluation methods regardless of the simulator selected.

Spectre Accelerated Parallel Simulator (APS) analog simulator provides Spectre accuracy with a 5X reduction in simulation time as compared to the original Spectre engine. Spectre X Simulator solves large-scale verification simulation challenges with up to 10X speed and 5X capacity improvements as well as scalable and massively parallel simulation for cloud computing. Spectre Extensive Partitioning Simulator (XPS) provides the FastSPICE high-performance and capacity simulation needed to handle memory and mixed-signal designs. The complete portfolio is rounded out by Spectre AMS Designer, Cadence's mixed-signal, mixed-language,

mixed-level, functional, behavioral, gate-level, and transistor-level simulator.

The Spectre RF Option provides accurate and fast simulation for RFIC circuits. The option includes periodic steady-state, small-signal, and noise analyses along with harmonic balance analysis capabilities to maximize performance without loss in accuracy. The Spectre

CPU Accelerator Option enables multi-thread simulation for transient and periodic steady-state analysis, which is extremely useful for verification of parasitic back-annotated designs across multiple CPUs. The Spectre Power Option is the dedicated transistor-level electromigration and IR drop (EM-IR) analysis built into the Spectre Simulation

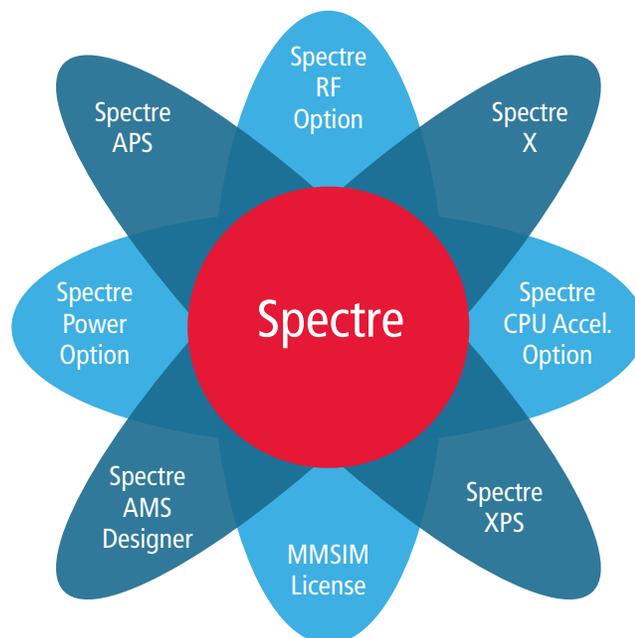


Figure 1: Spectre Simulation Platform

Platform and used as the analysis engine inside the Cadence Voltus™-Fi Custom Power Integrity Solution.

Cadence provides a unique multi-mode simulation (MMSIM) license that can enable any part of the platform on demand, so you can focus on simulating your design without worrying about which licenses are required for various simulation types.

Spectre Accelerated Parallel Simulator

Benefits

- Spectre APS is an enhanced version of the Spectre Circuit Simulator, providing the same golden accuracy for challenging analog, mixed-signal, and advanced-node post-layout designs with significantly faster simulation time.
- Spectre APS provides scalable performance, allowing users to take advantage of a multi-core hardware solver.
- Integration into the Cadence Virtuoso® ADE Product Suite provides simplified simulation for designers, including fast interactive simulation set up, powerful results visualization, and built-in measurements for post-processing of simulation results.
- Spectre APS is the analysis integrated engine into the Cadence Legato™ Reliability Solution, advanced device reliability analysis, Voltus-Fi Custom Power Integrity Solution, and EM-IR analysis
- Built on the Spectre Simulation Platform, enabling access to high-quality silicon-accurate, industry-standard, foundry-certified device models.
- Comprehensive set of circuit analyses covers all analog, RF, and mixed-signal domains.

Features

- Comprehensive circuit analyses supporting all of the classic Spectre Circuit Simulator analyses
- New post-layout simulation mode enables high-precision simulation for large post-layout designs and performs electromigration analysis

- Provides scalable performance with advanced parallel simulation on multi-CPU compute platform
- Comprehensive tools for statistical analysis
- Analyzes stability and identifies unstable and marginally stable feedback loops
- Accurate large signal noise analysis
- Behavioral Modeling with Verilog-A
- Native reliability, device aging analysis
- Built-in measurement with .measure and Spectre measurement description language (MDL)
- Advanced device modeling and support
- EM-IR analysis
- Static and dynamic circuit checks
- Data encryption
- Multi-technology simulation

Comprehensive circuit analyses across the platform

- DC: Operating point, DC match, DC sensitivity, and sweep analyses
- Small signal analyses: AC, noise, transfer function (xf), distortion (perturbation), AC match, AC sensitivity
- Analyze design stability with pole-zero analysis, loop stability analysis, and loop finder analysis
- RF analyses: Periodic and quasi-periodic steady state analysis, noise analysis and small signal analysis, and envelope analysis for modulated signals
- Transient analysis and transient noise analysis
- Native reliability analysis
- Co-simulation with Cadence Xcelium™ Parallel Logic Simulator for mixed-signal simulation
- Co-simulation with MathWorks Simulink
- Native support for parametric sweeps, corner analysis, and statistical analysis, including built-in fast Monte Carlo analysis (requires an additional license)

Post-layout simulation mode enables high-precision simulation and electromigration analysis

Spectre APS uses proprietary techniques to accelerate post-layout simulation. The post-layout simulation supports accelerated DC operating point calculation, an advanced matrix solver optimized for RC simulation and large matrices, and RC parasitic reduction. Multiple modes are provided to users that optimize set-ups for different applications, including custom IC simulation, analog IC simulation, and EM-IR analysis.

Comprehensive tools for statistical analysis

Spectre APS provides designers with the tools needed to analyze the effect of process variation on manufacturability and to reduce time to market at advanced process nodes. Traditional statistical analysis tools for corner analysis and Monte Carlo analysis are supported. Monte Carlo analysis has been enhanced with improved sampling methods to reduce the number samples required for converging to confidence interval. DC match and AC match analyses has been added to efficiently analyze local process mismatch effects and identify yield-limiting devices and parameters. Tight integration between Spectre APS and the Virtuoso ADE Product Suite offers a user-friendly interactive set-up, additional analysis capabilities such as Monte Carlo auto-stop, and advanced tools for visualization of statistical results. Fast Monte Carlo analysis from the Virtuoso Variation Option is now integrated natively into Spectre APS to allow batch-mode statistical analysis of standard cells.

Analyze stability and identify unstable and marginally stable feedback loops

Spectre APS provides stability analysis. Stability analysis can be used to simulate the loop gain and loop margin for either linear and periodic circuits. Stability analysis can be used for either single-ended or differential circuits. The loop finder feature was developed to supplement stability analysis and is used to identify which feedback loop in a multiple feedback loop is not stable or to find sources of marginal stability.

Accurate large signal noise analysis

Spectre APS provides transient noise analysis for large signal noise simulation. Transient analysis supports all noise types including thermal, shot, and flicker noise. To enable debugging the sources of circuit noise, noise injection from each device and each type of device noise is user controlled. Transient noise analysis results correlate well with linear and periodic noise analysis.

Behavioral modeling with Verilog-A

Spectre APS provides behavioral modeling capabilities in full compliance with Verilog-A 2.0. Verilog-A modules can be compiled for optimum simulation performance. Implementation is optimized for compact device models, offering comparable performance to built-in device models.

Native reliability and device aging analysis

Spectre APS provides native device reliability analysis. Users can simulate the degradation of device characteristics as a function of the circuit operation conditions and time. The native device aging analysis is used inside of the Legato Reliability Solution to analyze the interaction of device aging with process variation and device self-heating.

Built-in measurement with .measure and Spectre MDL

Standard SPICE measurement functions (.measure) are supported. In addition, Spectre APS offers the Spectre measurement description language (MDL) to simulation measurements and to automate standard cell library characterization. Spectre MDL enables the designer to post-process simulation results, make measurements, and tune the simulator to provide the best performance/accuracy tradeoff for a specific measurement.

Advanced device modeling and support

Spectre APS supports MOS, BJT, specialty transistor models, resistors, capacitors, inductors, transformers and magnetic cores, lossy and lossless transmission lines, independent and controlled voltage and current sources, and Z and S domain sources. Spectre APS provides a user-defined compiled model interface (CMI). It allows for the rapid inclusion of user-

defined models for a “model once, use everywhere” capability.

EM-IR analysis

Spectre EM-IR is a transistor-level electro-migration and IR drop (EM-IR) tool based on a patented voltage-based iteration method and can be used with Spectre APS. Two analysis options are provided: direct method, high accuracy, and iterated method, high capacity. This analysis provides best-in-class transistor-level EM-IR accuracy, especially in advanced-node FinFET processes. It uses Cadence’s patented voltage-based iteration method, which requires a smaller memory footprint and runs faster than the industry’s traditional current-based iteration method.

Asserts and circuit checks

Spectre APS provides tools to monitor device operating conditions or check for common design problems, such as high impedance nodes, leakage paths, or power consumption problems. Spectre assert checks monitor design or model parameters, element or subcircuit terminal currents, element or subcircuit terminal voltages, or operating point parameters for violations of user-defined conditions. Circuit checks are provided to check for more complex circuit problems, such as identifying floating nodes or leakage paths. Two types of circuit checks are provided, dynamic checks and static checks. Dynamic checks are performed during transient simulation while static checks are performed during parsing.

Specifications

Comprehensive list of analog device models supported

- Advanced-node models, including the latest versions of the BSIM CMG, BSIM IMG, and UTSOI models
- MOSFET models, including the latest versions of the BSIM3, BSIM4, BSIM Bulk (BSIM6), PSP, and HiSIM
- High-voltage MOS models, including the latest versions of the HiSIM HV, MOS9, MOS11, and EKV
- Silicon-on-insulator (SOI), including latest versions of BTASOI, SSIMSOI, BSIMSOI, BSIMSOI PD, and HiSIM SOI

- Bipolar junction transistor (BJT) models, including the latest versions of VBIC, HICUM, Mextram, HBT, and Gummel-Poon models
- Diode models, including the diode, Phillips level 500, and CMC diode models
- JFET models, including the JFET, Phillips level 100 JFET, and Individual dual-gate JFET models
- IGBT models, including PSpice® IGBT model and HiSIM IGBT models
- Resistors, including linear resistor, diffused resistor, CMC two-terminal and three-terminal resistor, and physical resistor models
- GaAs MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov
- GaN MESFET models, including Angelov, ASM, and MVSG models
- Silicon TFT models, including RPI Poly-Silicon and Amorphous Silicon Thin-Film models
- Verilog-A compact device models
- Z and S domain sources
- User-defined compiled model interface (CMI), allowing for the rapid inclusion of user-defined models
- Josephson Junctions
- Specialized reliability models (AgeMOS) for simulating the effect of HCI and BTI
- Miscellaneous power models, including the relay, transformer, non-linear magnetic core, and winding
- Miscellaneous RF models, including the DC block, DC feedthrough, and microstrip and stripline elements (bend, cross, corner, curve, open line, tee models)

Language and netlist support

The netlist formats, behavioral modeling languages, parasitic netlist formats, and stimulus files are common across the Spectre Simulation Platform. Supported formats include:

- Spectre and SPICE netlist formats
- Spectre, SPICE, and PSpice models

- Verilog-A 2.0 LRM-compliant behavioral models and structural netlists
- DSPF/SPEF parasitic formats
- S-parameter data files in Touchstone, CITI-file, and Spectre formats
- SST2, PSF, PSF XL, and FSDB waveform formats
- Digital vector (VEC), Verilog-Value Change Dump (VCD), Extended Verilog-Value Change Dump (EVCD), and digital stimulus

Platform support

- x86 64-bit Red Hat Enterprise 6.5 (and higher) and V7, SLES 11 and 12
- Commercially available cloud solutions

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.

- More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.



Cadence software, hardware, and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's Intelligent System Design strategy helps customers develop differentiated products—from chips to boards to intelligent systems. www.cadence.com

© 2019 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. SystemC is a trademark of Accellera Systems Initiative Inc. All other trademarks are the property of their respective owners. 12991 08/19 SA/RA/PDF