

# CADENCE SPACE-BASED ROUTER

As designers integrate more and more digital and analog/mixed-signal content into single chips, they face critical effects on yield and manufacturability, such as growing lithography issues, inconsistent manufacturing rules, copper materials, electrical concerns, and performance requirements. Cadence® Space-Based Router addresses all of these concerns simultaneously, helping designers achieve shorter time to convergence, better quality of silicon, and differentiated products for consumer and wireless markets.

## CADENCE ROUTING TECHNOLOGY

The physical implementation process—including routing—is what can make or break your yield and manufacturing objectives. Shapes on the layout not equal to the shapes on the silicon means costly silicon re-spins. To compensate, designers rely on resolution enhancement techniques and density management techniques. They also employ overly conservative rules which result in a die area penalty.

Cadence Space-Based Router has the capacity and flexibility to help you manage these complex issues simultaneously, greatly reducing mask re-spin costs. Its unique routing architecture is based on a patented space-based approach that meets the manufacturing, lithography, materials, and performance requirements of high-end digital and analog/mixed-signal designs. The router works seamlessly within both the Virtuoso® custom design and Encounter® digital design platforms for maximum productivity and quality of silicon.

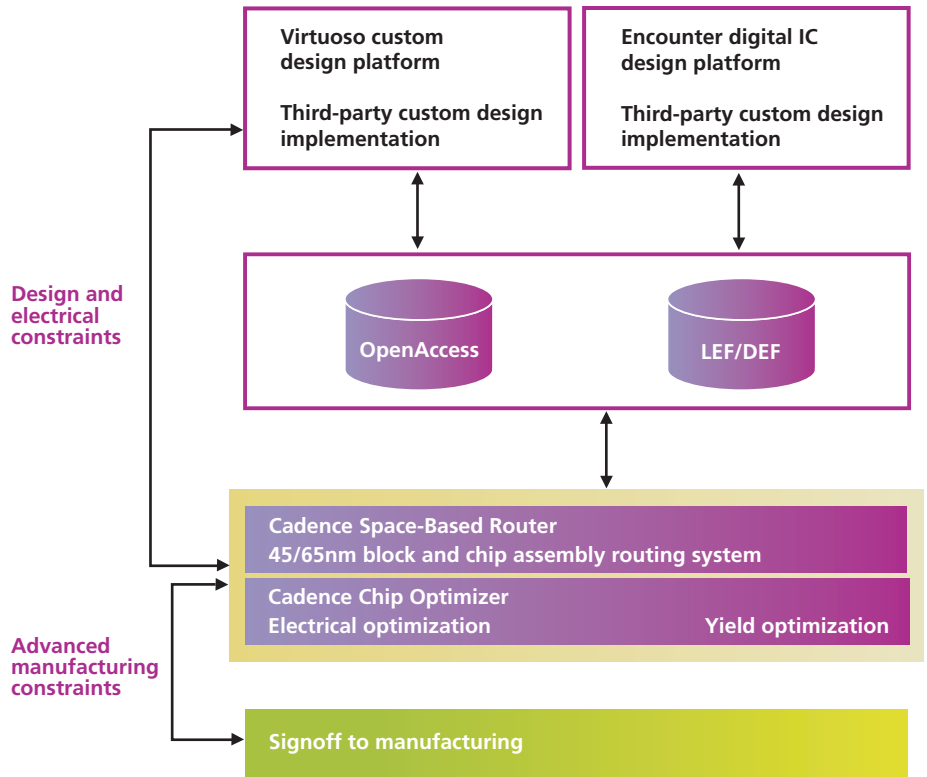


Figure 1: Cadence Space-Based Router's architecture incorporates electrical and manufacturing constraints to achieve optimal quality of results for mixed-signal and high-performance designs

## CADENCE SPACE-BASED ROUTER

Cadence Space-Based Router is a silicon-proven, three-dimensional, hierarchical, grid-less, space-based, full-chip and block routing convergence system for advanced mixed-signal, analog, and custom digital designs at 65nm and below. Its constraint-driven, interactive/automatic physical design interconnect environment offers a streamlined flow, from constraint definition and routing through analysis/verification and refinement.

The router models advanced processes and design constraints, providing maximum chip control and exceptional results upfront in the design process for high-performance blocks and full chips. It also features specialty mixed-signal routing, incremental in-core electrical analysis, and design-for-manufacturing and design-for-yield optimization.

Cadence Space-Based Router improves the design's manufacturability and reduces time-consuming post-processing for OPC and copper planarity issues, ensuring that you meet your manufacturing and electrical objectives the first time around. You can specify advanced constraints

for high-performance routing such as sophisticated wire tapering, layer control, and noise avoidance. Complex pre-routes, previously done manually, can now be performed automatically. The router sets the standard for incremental and flexible design editing and routing—you can modify shapes, nets, and regions easily, and each step in the flow is re-entrant.

## BENEFITS

- High capacity easily handles flat and hierarchical data for 250K net designs
- High-performance multi-threaded implementation accelerates completion of the largest designs
- Innovative hierarchical, 3-D, space-based architecture enables accurate modeling, manipulation, and checking of sophisticated geometries and constraints for sub-65nm interconnect design closure
- Sign-off-quality advanced design-rule interconnect checking system delivers correct-by-construction design closure
- Preserves the art of precision hand-crafting while offering the benefits of automation

- Offers an intuitive and easy-to-use interactive and automatic interconnect environment
- Advanced collaboration features allow engineers to communicate better through the use of annotations and snapshots
- Uses flexible and open systems such as OpenAccess, TCL, and XML

## FEATURES

### INTERCONNECT CLOSURE

- Gridless, space-based routing for optimal quality of results
- 3-D global router produces real interconnect for accurate modeling of wire lengths and via counts
- Corridor router for fast convergence
- Specialty routing capabilities such as differential pair, shielding, and bus routing
- Feature-rich power router
- Connectivity and design rules are omnipresent for correct-by-construction automatic routing/interactive editing
- Highly incremental interactive and automatic routing to complete netlist changes or to work from pre-routed designs
- Wire push capability “pushes” neighboring wires to fit a new wire optimally and still meet design rules
- Built on an electrically- and manufacturing-aware platform
- Shares a common platform with the Cadence Chip Optimizer for highest yield

### INTERCONNECT CHECKING

- Supports sophisticated recommended rules and constraints at 65nm and below
- Hierarchical, shaped-based, sign-off quality checking on the interconnect layers

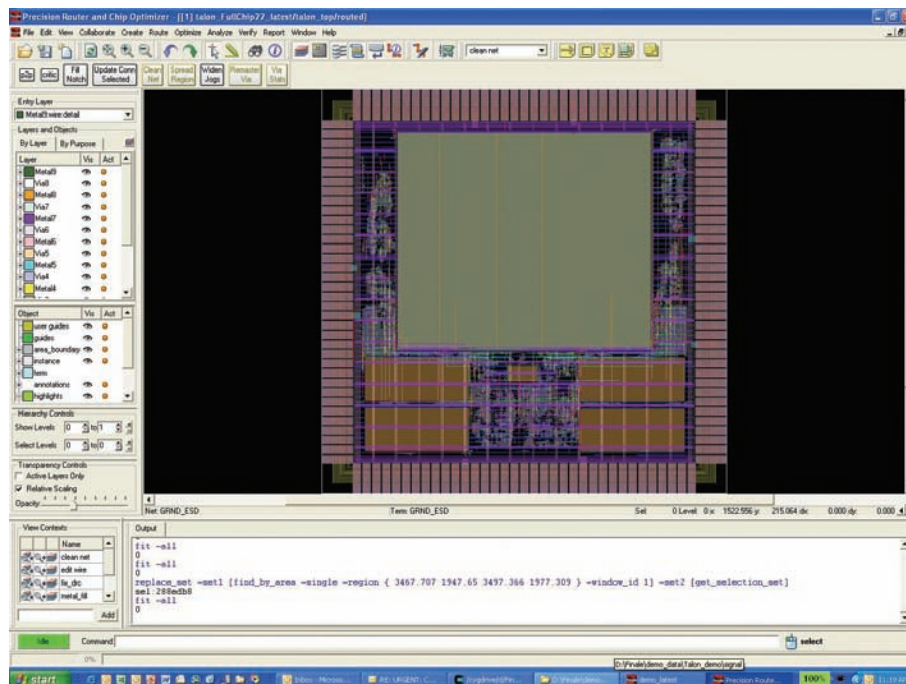


Figure 2: A modern, intuitive, user-configurable, and easy-to-use interconnect synthesis environment supports comprehensive design annotation and collaboration features

- Fast and highly accurate interactive DRC and connectivity (open/short) checking
- Create derived layers by performing Boolean and sizing operations
- Browser to analyze verification results (including results from third-party tools)

## UNPARALLELED SPEED AND HIGH CAPACITY

- Uses new (patented) hierarchical modeling and search algorithms
- High-performance multi-threaded implementation and operation

## FULL-FEATURED NAVIGATION SYSTEM

- Aerial View window provides full-chip navigation context
- Query engine enables powerful searches of layout data
- Fully tune the desired layers, layer purposes, and transparency for display and selection
- Useful views and environment contexts can be bookmarked and saved
- Pan and zoom dynamically
- Traverse hierarchy levels
- Hierarchical Cycle Select uncovers all object types and layers under the cursor
- Search and highlight instances and nets

## INNOVATIVE PROJECT COLLABORATION

- Create annotations and notes including text (plain and callouts), arrow, rectangle, and dimension overlay shapes
- Export/email JPEG and PNG graphic files and annotations for review
- Annotation browser with auto-navigation and bind-key support
- Automatic JPEG context capture
- Annotation sharing

## EASY TO LEARN, USE, AND EXTEND

- Intuitive windowing system and command set
- Extensive TCL programming interface for command and rule scripts and replay sessions
- Control layer and object display with Open GL-based transparency
- Create bind-keys for one-key execution
- Save and exchange information with XML

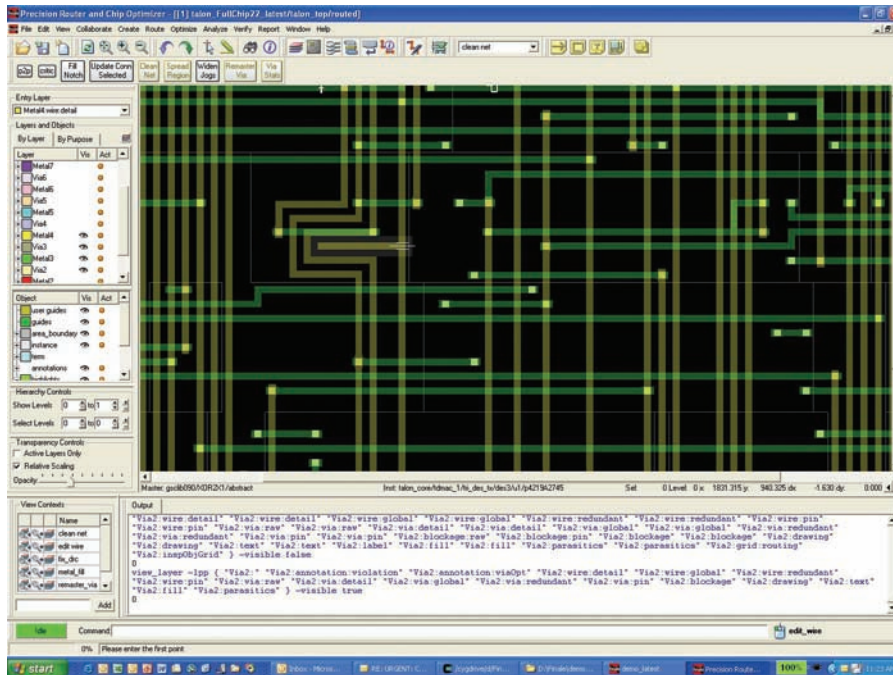


Figure 3: Comprehensive support for interactive editing and routing includes push/shove, rule halos, and source/target alignment for surgical precision of design and manufacturing convergence

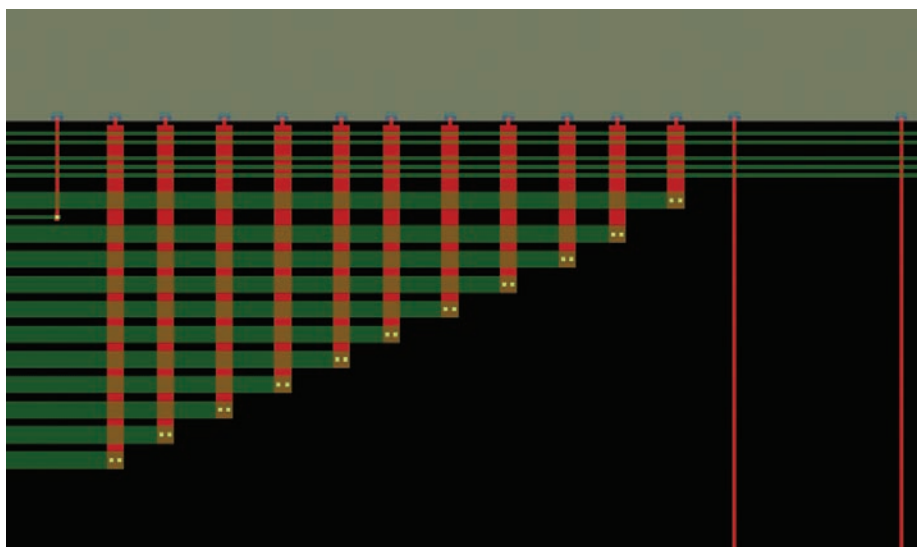


Figure 4: Advanced design and manufacturing features such as variable widths and spacings, pin tapering, and recommended via patterns enable automated design convergence and high yield

## SPECIFICATIONS

### PLATFORM/OS

- Sun Solaris (32-bit, 64-bit)
- Linux (32-bit, 64-bit)
- IBM AIX (32-bit, 64-bit)

### INTERFACES

- Input
  - OpenAccess, XML, LEF DEF, GDSII, CDB, SPEF, timing libraries and constraints
- Output
  - OpenAccess, XML, LEF DEF, GDSII

### INTEROPERABILITY

#### Cadence Chip Optimizer

- Addresses both DFY and DFM issues much earlier in the design flow
  - Speeds geometric, electrical, and manufacturing convergence
  - Improves design margins and reduces guard-banding
  - Eliminates convergence iterations with electrically correct design
  - Delivers faster, more reliable ramp-to-volume silicon with up to six points of yield improvement
- Handles the most sophisticated geometries and constraints
  - Enables accurate and precise modeling and optimization with a true hierarchical, 3-D, space-based approach

- Handles complex and tiered rules and constraints at 90nm and below
- Ensures the greatest manufacturability and performance gains with powerful topological changes
- Silicon-proven on high-volume, high-performance silicon at 180, 130, 90, and 65nm process nodes
- Easy to adopt
  - Works seamlessly with the Encounter digital design and Virtuoso custom design platforms
  - Works with third-party implementation flows through industry-standard interfaces
  - Runs natively on OpenAccess

#### Virtuoso XL Layout Editor

- Accelerates block authoring through connectivity-driven features and flow (schematic or netlist)
- Promotes a correct-by-construction layout to reduce verification iterations
- Increases productivity and design quality with constraint- and design-rule-driven features
- Automatically ensures real-time design and process correctness
- Simplifies and optimizes device generation with the new menu-driven QuickCell feature of the standard SKILL-programmable parameterized cells
- Efficiently plans, places, and routes large block designs with custom floor-planning, automatic placement, and accelerated interactive routing features

#### Virtuoso Chip Editor

- Reduces time to market with increased layout productivity
- Provides high performance and high capacity to handle the largest designs
- Minimizes training requirements by retaining the look and feel of Virtuoso Layout Editor
- Expedites engineering change orders for complex digital and mixed-signal designs using SoC Encounter™ round-trip editing
- Reduces design cycle time by providing chip-planning capabilities and minimizing data translation steps

## CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or internet — they can also provide technical assistance and custom training
- SourceLink® online customer support gives you answers to your technical questions — 24 hours a day, 7 days a week — including the latest in quarterly software rollups, product release information, technical documentation, software updates, and more
- Cadence-certified instructors teach more than 80 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

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