

Liberate Trio Characterization Suite

Industry's first complete library characterization system optimized for the cloud

The Cadence® Liberate™ Trio Characterization Suite delivers the industry's most comprehensive and robust solution for the characterization, variation modeling, and validation of your foundation IP—including standard cells, I/Os, and complex multi-bit cells. Its cloud-ready technology is scalable to thousands of cores for high throughput and employs advanced machine-learning techniques to determine critical corners for characterization.

A Complete Solution

The Liberate Trio Characterization Suite offers high-performance characterization, process variation modeling, and validation of standard cells, custom cells, multi-bit flip-flops, and I/Os. The suite achieves accuracy and high speed through the powerful combination of the "Inside View" approach—patented technology for generating and optimizing characterization stimulus—and a parallel processing capability that takes advantage of enterprise-wide compute resources and a simplified flow to deal with enormous collections of corners across libraries. The Liberate Trio suite is a one-stop shop for all aspects of standard-cell library characterization (Figure 1).

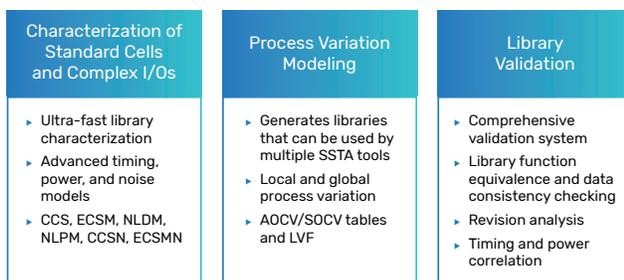


Figure 1: The Liberate Trio suite brings together all aspects of characterization for standard cell libraries

Benefits

- ▶ Ultra-fast cell library characterization for standard cells and complex I/Os for low-power and/or high-speed designs
- ▶ Automatic pre-characterization of each cell using the Inside View transistor-level circuit analysis technology to learn all internal logic states and enable automatic vector generation
- ▶ Ultra-fast throughput to complete library validation overnight on a small number of multi-core computers
- ▶ Variation-aware timing model creation accounting for process variations (systematic and random) for any set of correlated or uncorrelated process parameters
- ▶ Utilizes a single script to configure generation of all PVT corners in a library, including corner-specific settings and library content
- ▶ Statistical and nominal libraries are unified in a single characterization run
- ▶ Ensures that all corner libraries have the identical structure required for static timing analysis (STA) scaling

- ▶ Provides restart and re-characterization of a full set of libraries
- ▶ Provides critical corner prediction using machine learning
- ▶ Runtime performance and results monitoring in a single GUI cockpit

Comprehensive Library Characterization System

The Liberate Trio suite features the industry’s first complete library characterization system (Figure 2) to enable faster performance and better accuracy with:

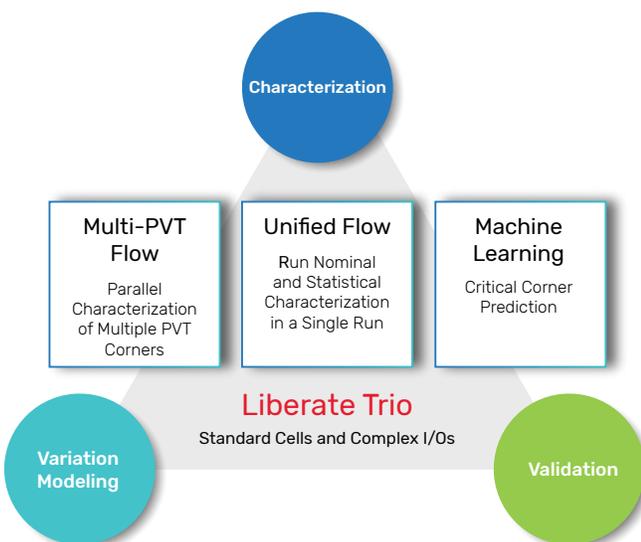


Figure 2: The Liberate Trio unified library characterization system

- ▶ Performance improvements through multi-PVT flow and unified flow
- ▶ Cloud enablement with massive distribution and parallelization algorithms
- ▶ Critical corner prediction using machine learning
- ▶ Enhanced GUI cockpit

The throughput of a library characterization project is determined by the efficient utilization of compute resources. By treating a characterization project as a single task, redundant analysis and underutilized clients can be removed.

Library database management is further simplified through the Liberate Trio suite with accurate corner selection, improved characterization efficiency, and automation of validation and correlation functions to scale with ever-increasing library project requirements.

By using existing library corners, new voltage-scaled corners can be generated without additional characterization through a new smart interpolation feature. The Liberate Trio suite leverages cloud resources for an enormous collection of libraries and reduced characterization time for large libraries from weeks to days.

Characterization of all cells in all corners can now be launched from a single script and monitored using an enhanced GUI cockpit with the Liberate Trio suite. Modeling attributes extracted from standard cell circuit analysis are shared among all corners to reduce runtime and ensure the structural symmetry needed for STA scaling applications.

Characterization

The Liberate Trio suite can generate electrical cell views for timing, power, and signal integrity, including advanced current source models (CCS and ECSM).

Our Inside View approach automatically pre-characterizes each cell using transistor-level circuit analysis, which yields all the necessary stimulus and internal logic states to ensure a complete, accurate, and highly efficient characterization of that cell (Figures 3 and 4).

The Liberate Trio suite supports complex cells, including those required for high-speed and/or low-power design such as pulse latches, multi-bit flip-flop arrays, custom cells, state retention flip-flops, level shifters, power switches, and cells with sleep modes.



Figure 3: Pre-characterization circuit analysis

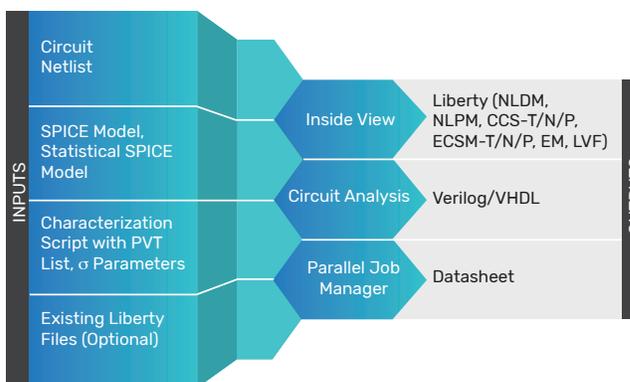


Figure 4: The Liberate flow with multiple clients demonstrating parallel characterization

Multi-PVT Flow

With every new node, designers face the challenge of characterizing an enormous number of corners. The Liberate Trio suite addresses this challenge with a multi-PVT flow that characterizes multiple corners in parallel. The resulting libraries maintain consistency in structure. Liberate clients in the multi-PVT flow will boost library characterization efficiency by 70%.

Multiple PVT corners of the same library are run simultaneously across many Liberate clients using identical vectors to reduce the total time to generate results.

Process Variation Modeling

The Liberate Trio suite also provides an ultra-fast characterization of process variation-aware timing models. It generates libraries that can be used with multiple statistical static timing analyses (SSTAs) without requiring re-characterization for each unique format. Its statistical characterization also generates advanced on-chip variation (AOCV) tables, statistical on-chip variation (SOCV) tables, and Liberty Variation Format (LVF).

The Liberate Trio suite calculates non-linear sensitivity, accounting for systematic and random variation for any set of correlated or uncorrelated process parameters. The resulting libraries can be used to model both local (within-cell and within-die) variations and global die-to-die variations.

SSTA provides a more realistic estimation of timing relative to actual silicon performance, often reducing worst-case timing margins by 10-15%, resulting in a higher performing, higher yielding silicon.

To accurately predict variation, SSTA needs variation-aware timing models that account for both systematic process variations (due to lithography) and random process variations (due to doping fluctuations between transistors).

Unified Flow

Statistical libraries in LVF and nominal libraries are now generated using a unified characterization run that shares statistical and nominal SPICE process models. This flow eliminates the need to merge libraries at the end of a statistical run, and the combined characterization run improves performance.

Critical Corner Prediction

The Liberate Trio suite leverages clustering techniques from machine learning to identify and predict critical corners based on a handful of cells as opposed to a complete library. Given a range of voltages, the voltage corners needed for characterization can be predicted while maintaining accuracy of analysis. This feature significantly reduces the number of libraries that need to be characterized.

Validation

Liberate Trio validation provides a collection of utilities for validating libraries including functional equivalence checking, data consistency checking, revision analysis, and correlation with various electrical analysis tools for timing, noise, and power (Figure 5).

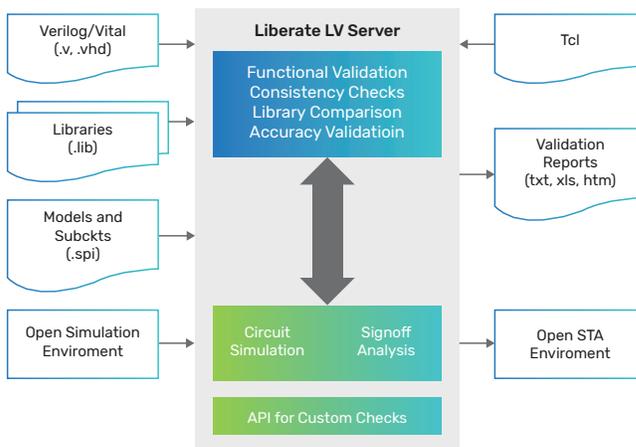


Figure 5: Library validation inputs and outputs

Using the Liberate Trio suite, complete validation of a library can be achieved overnight on a small number of multi-core computers. For library providers, this ensures library quality before the library is shipped. For library users, it allows cross-checking of the incoming library and provides a clear understanding of the impact of any changes due to revisions of extracted cell netlists or process models.

Library characterization requires a complex combination of circuit simulations, data measurements, data collection, and formatting—often distributed across a large computer network. Since each library view is used for multiple chip designs, it is paramount that the library data is correct and not undermined by measurement inaccuracies or incorrect user input. The Liberate Trio suite provides the means to validate and verify the final library, ensuring consistency, completeness, and accuracy.

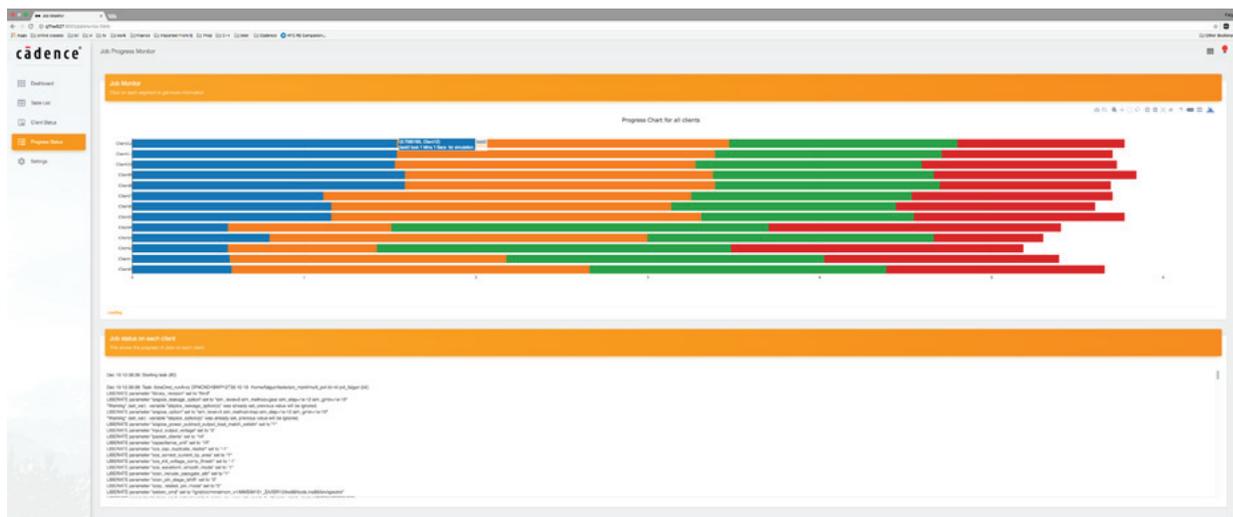


Figure 6: A new GUI dashboard reports runtime performance, status, and results

Characterization Job Monitor GUI

A brand-new characterization job monitor GUI is available with the Liberate Trio suite to monitor the progress of the characterization runs. It provides real-time runtime metrics for each library characterized per corner, cell, data type, etc. Users have access to data analytics from the run and can analyze the data to look at all aspects of the characterization run. Figure 6 shows the new Liberate GUI dashboard that reports runtime, performance, status, and results.

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