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Improving Test Coverage and Eliminating Test Escapes Using Analog Defect Analysis

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While the analog and mixed-signal components are the leading source of test escapes that result in field failures, the lack of tools to analyze the test coverage during design has made it difficult for designers to address the issue. In this white paper, we explore the methodology for performing analog fault simulation of test coverage based on defect-oriented testing. In addition, we look at how the Cadence® Legato™ Reliability Solution can be used to calculate test coverage and demonstrate the feasibility of the solution on a practical design, enabled through an advanced fault simulation engine.

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Introduction

There might be a tendency to think that a design is done once the tapeout is complete, or once characterization of the first samples on the bench is complete. However, the reality is more complex. Oftentimes, design projects live on well beyond the time when designers would like them to as the process of debugging field failures begins. Changing this dynamic has become more important as designers focus more on mission-critical applications like automotive design.

Let's consider a simple example. Suppose that, in production, the failure rate for an automotive design is 1 defective part per million (dppm). This number seems pretty good. So, what would the impact on automotive production be if all the chips in a car had the same 1dppm failure rate? For a typical mid-class case, 1dppm for the ICs translates into 300dppm for the electronic control units (ECUs) in the car. This ECU failure rate means 15,000 defective cars per million cars produced, a failure rate of 1.5%.[1] Automobile manufacturers would not be happy if more than 1% of the cars coming off the production line did not work.

The impact of even a 1dppm failure rate helps explain the requirement from suppliers for 0dppm for automotive components. Digging in a little deeper, it has been reported at test conferences that between 80% to 95% of field failures are due to the analog or mixed-signal portion of products with the remainder of field failures due to interconnect, memory, or digital. The takeaway is that the automotive ICs must have low failure rates and reducing the number of analog field failures is the best place to focus efforts. While digital designers have access to many tools to analyze and insert test into a design, analog designers have had few tools to support analog test.

Simulating Analog Test

It would be helpful if there was an analog equivalent of the automatic test insertion, boundary scan, etc., tools that digital designers use today. While these types of tools do not exist for analog designs, analog designers can take advantage of a tool that the digital designers have long used—fault simulation. Analog fault simulation has been proposed for many years[2, 3], but the technology has not proliferated.

For digital circuits, relatively simple fault models stuck at 0 (st0) and stuck at 1 (st1) have proved sufficient for analyzing fault coverage. For analog designs, defining faults has proved to be much more of a challenge. Certainly, st0 and st1 are not sufficient, but what is sufficient? Are faults catastrophic, that is, shorts and opens? Are faults parametric? Do faults exist for primitive devices? Do they exist for circuit primitives: current mirrors, differential pairs? The lack of analog fault models has proved to be a challenge when trying to define a methodology for simulating test coverage.

Defect-Oriented Test

The solution to the difficulty of defining analog faults has been to refine the problem. Instead of undefinable analog faults, we model manufacturing defects and simulate their effect on the circuit. Defect-oriented test evaluates the ability of the test program to identify and eliminate manufacturing defects[4]. From studying manufacturing processes, standard defects can be identified. Once a list of defects has been compiled, models for the defects can be defined. Then the design in the test fixture can be simulated using the test program including the defects one at a time. The simulation results can be compared to the test limits and a decision made whether the defect has been detected or not based on whether the test passed or failed. The results for each test can be tabulated, as well as the overall test results. The individual test results provide insight into the effectiveness of the individual tests. The overall test results provide the test coverage for the test program.

Currently the IEEE P2427 Working Group is standardizing the definitions of manufacturing defects for analog simulations. An example of some the defect models is shown in Figure 1.

Defect category	Equivalent Defect Abstraction	Comment
DC Short, same layer and in between layers	R_f	Resistance with Rf value given as a parameter, technology dependent and will become a part of defect coverage report
DC Open, general case	$Z_f = \frac{R_f}{1+j\omega R_f C_f}$	Resistance and capacitance given as parameters, technology dependent and will become a part of defect coverage report
DC Open Transistor Gate	$V_{gs}=k \cdot V_{ds}$ $k = \frac{C_{gdo}}{nWLC_{ox}}$	KU Leuven & ON -Semi ITC 2016 Reference [1]
AC Coupling, same layer and in between layers	C_f	Capacitance C_f given as a parameter, technology dependent
Resistive Bridge (short)	R_f	Resistance with Rf value given as a parameter, technology dependent and will become a part of defect coverage report
Resistive Bridge (open)	$Z_f = \frac{R_f}{1+j\omega R_f C_f}$	Resistance and capacitance given as parameters, technology dependent and will become a part of defect coverage report

Figure 1: Example of proposed defect models from the IEEE P2427 Working Group

In more detail, a defect is a failure in a design intent element; for example, a poorly formed contact prevents the metal of the VDD net breaks from making contact to the drain terminal of a device so defects are shorts or opens. A fault occurs when a circuit fails to meet specification; for example, an operational amplifier has excess offset voltage.

Example of Device Defects

Let's look at a simple example of how to apply these defects. Consider a single n-channel MOSFET transistor, shown in Figure 2. The source and bulk are shorted, so the device has three terminals: drain, gate, and source. For transistor, each terminal may be open for a total of three opens. For junction, gate drain, drain source, and gate source, there can be a short for a total of three shorts. As a result, when we simulate device defects, each MOS transistor will have six possible defects to simulate. One note is that the IEEE P2427 Working Group has defined special models for open-gate defects, so these are not modeled the same as the open-drain and open-source defects.

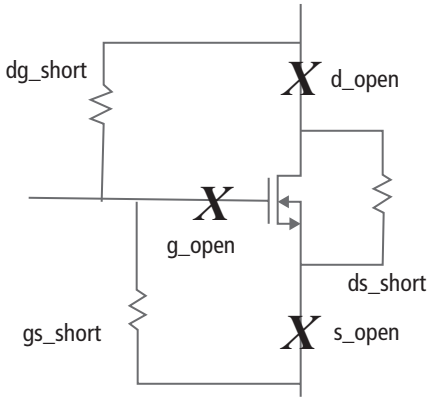

Figure 2: N-channel MOSFET with manufacturing defects

Defects for other devices such as resistors, capacitors, bjts, and diodes can be defined in a similar manner. Defining defects for interconnect can also be performed. The simplest approach is to perform parasitic extractions and replace every parasitic resistor with an open defect and every parasitic capacitor with a short defect.

Methodology for Analog Defect Simulation

The methodology for simulating the test coverage is the three-step process shown in Figure 3. The first step is to identify all the potential defects in the design using the rules discussed earlier. Once the defect list or defect universe has been compiled, then each defect needs to be simulated. The defects are simulated using manufacturing test conditions and captured in simulation testbenches. The simulation results are compared to the test limits. If the test failed, then the test program detected the defect. We tabulate the defect test results and determine the test coverage.

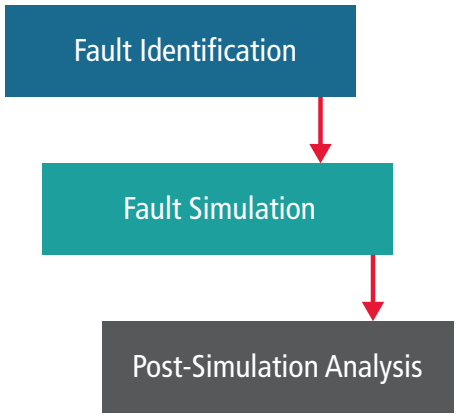

Figure 3: Methodology for simulating test coverage

The methodology for simulating analog test has been demonstrated[4]; however, it has not been fully automated. In addition, current implementations exist outside of the analog design flow. The result is that adopting existing approaches requires significant changes to the design methodology and results in the need to re-qualify the design flow.

Using Analog Defect Analysis

Digital designers have access to a rich set of tools for design for test (DFT) including the ability to automatically insert support for test during synthesis and cell-aware test, to build the fault dictionary. As a result, they often perform fault analysis on the layout database. For example, fault analysis of digital mini-cells libraries is based on the extracted netlist. However, analog designers do not have DFT tools. If analog designers wait until the layout is complete before considering the testability of the design, they are faced with the likelihood of having to rework their design to make it testable. Experience has shown that the better approach for analog designers is to adopt an in-design approach (such as electrically aware design, integrated physical verification system, or design for manufacturing (DFM)) to analyzing how testable their design is so they can modify it before starting layout. This requires a tradeoff of early visibility into potential test issues against the capturing every little detail of the defect coverage.

Extracting the defects from the layout can still be used for the final verification and provides insight into two effects. The first effect is potential parametric variations due to a defect. For example, assume that a transistor has 10 fingers. Depending on the layout, anywhere from 0 to 10 fingers may actually be in operation. The second effect is the potential functional failures due to shorts at a higher level of the design hierarchy. For example, the inputs of an operational amplifier are shorted. In this white paper, we focus on schematic-level defect simulation to enable in-design analysis of the test coverage because this approach provides designers with insight into how testable their design is and how to improve the testability of their design.

A New Approach to Analog Defect Simulation

In response to the need for a more systematic approach for analyzing analog test coverage, Cadence developed the Legato Reliability Solution to support analog defect simulation. The Legato Reliability Solution is built on the Cadence Virtuoso® custom IC design platform and Spectre® Accelerated Parallel Simulator (APS) to automate simulation of analog test coverage and incorporate analog defect analysis into their methodology with a little change to their flow. It provides analog defect analysis that can evaluate an analog test's ability to identify manufacturing defects and report the defect coverage of the test, enabling analog designers to reduce testing costs and minimize test escapes.

Integrating the solution into the standard analog design test flow reduces the learning curve. In addition, adoption of the solution has minimal impact on the design flow, meaning it requires little flow qualification. For designers, the difference is whether the faults (defects) are extracted from the schematic or from the layout (extracted view). By simulating the test after the schematic-level design is complete, the designer can simulate the coverage based on devices. This information is useful for understanding test coverage for each block and allowing the designers to increase the observability of the faults (defects) in the block by inserting additional test points or an analog test bus.

Defect Identification

The first step in analyzing analog test is to create a list of potential defects for simulation. The list consists of the defect definition including the defect type, an open terminal or short connecting ether device terminals, the nodes affected by the defect, and the value of the defect. Doing a quick calculation for a typical IP block like a fractional-N PLL, there are about 20,000 transistors. If there are 6 defects per transistor, then the defect list will contain more than 100,000 defects. Given the large number of defects in even small blocks, manual creation of a defect list is not possible.

The Legato Reliability Solution includes an Assistant tool that automatically generates the defect list for simulation. In the example shown in Figure 4, for all MOS devices in the netlist, one must create bridge defects with a value of 1Ω resistor to short the terminals defined in the Pin Name(s) list. Because the drain [D], gate [G], and source [S] pins are named, defects shorting the node pairs D-S, D-G, and S-G are generated. In this example, the block is small so only 19 defects are identified. The Assistant provides various filters so designers can focus on testability of different parts of the design, which is useful when simulating complex blocks, such as a fractional-N PLL.

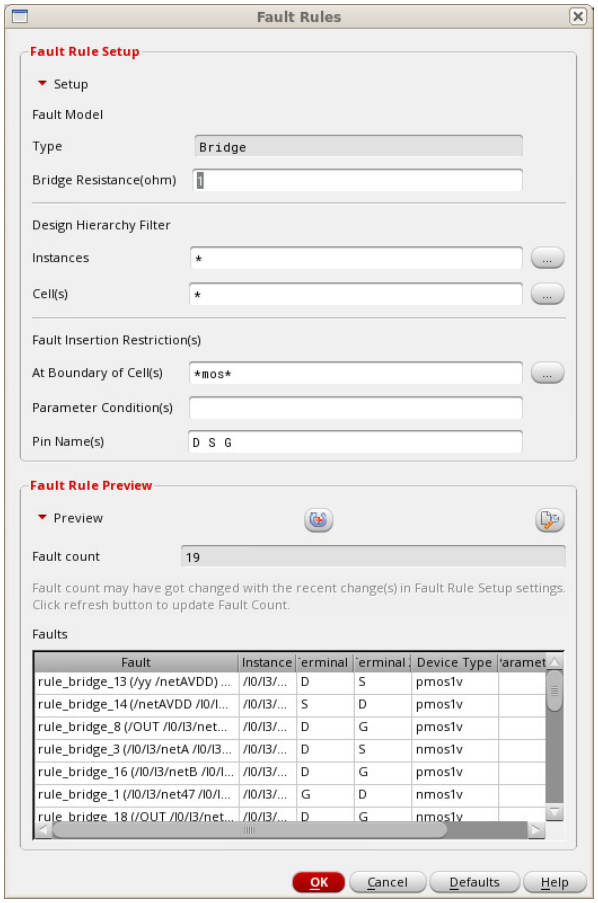

Figure 4: Virtuoso ADE Assembler fault assistant

Designers can either create global rules using wildcards, or they can create detailed rules for each type of manufacturing defect. The rules file can be saved and shared so every member of the design team or every PDK user uses the same set of rules for generating the defect list for simulation. The fault list is automatically minimized by built-in rules for defect collapsing. For example, suppose a transistor is diode-connected, that is, the gate and drain are shorted. In that case, the gate-drain short defect is not generated. So, the defect list is correct by construction and includes the minimum number of defects.

Defect Simulation

The Legato Reliability Solution analog defect simulation takes advantage of the Spectre APS analog fault simulation engine. The Spectre APS analog fault simulation can be used for various applications requiring simulation of defects for analog test—the focus of this whitepaper—and other applications like analog functional safety simulation. Spectre APS analog fault simulation supports two simulation modes: direct fault analysis (DFA) and transient fault analysis (TFA). The Spectre APS analog fault simulation engine is also available when performing mixed-signal simulation using Spectre AMS Designer for simulation of faults in the analog partition of the simulation.

Let's review some basic assumptions about defect simulation. In defect simulation, we are trying to replicate analog test. The test flow is that:

1. The loadboard is configured for the test, relays on the loadboard are energized so the appropriate test equipment, then loads, etc. are connected to the device under test
2. The test stimulus is applied
3. Measurements are made, for example, a voltage measured at a strobe point, the timing of a voltage crossing, etc.

4. For static measurements such as static power supply current, the measurements may be made several times and the results averaged to reduce the effect noise on the measurement. For dynamic measurements such as slew rate, steps 2 and 3 can be repeated and the results averaged to reduce the effect of noise on the measurement.

When simulating, the test conditions are replicated. Fortunately, the simulation only needs to be performed once.

Managing the number of defect simulations can be challenging. There are several approaches available to designers including fault collapsing, distributing the simulations, advanced sampling techniques, and TFA, among others.

DFA

In the direct fault analysis (DFA) mode, the faults are inserted into the nominal design at the beginning of the simulation analysis, i.e., transient, DC operating point, AC small signal. This mode provides the most accurate results and the most complete description of defect's effect on the circuit's performance. The DFA mode also serves as a reference to verify the effect of defects on the circuits. However, when the number of faults is large, the simulation time can become impractically long. Spectre APS DFA is supported within the distributed simulation mode to address this problem.

Figure 5 illustrates DFA where the green waveform is related to nominal circuit, and the blue one is with a fault inserted. DFA allows the designer to estimate the deviation between these two at the specified strobe points, or at each simulation step using device checkers or asserts.

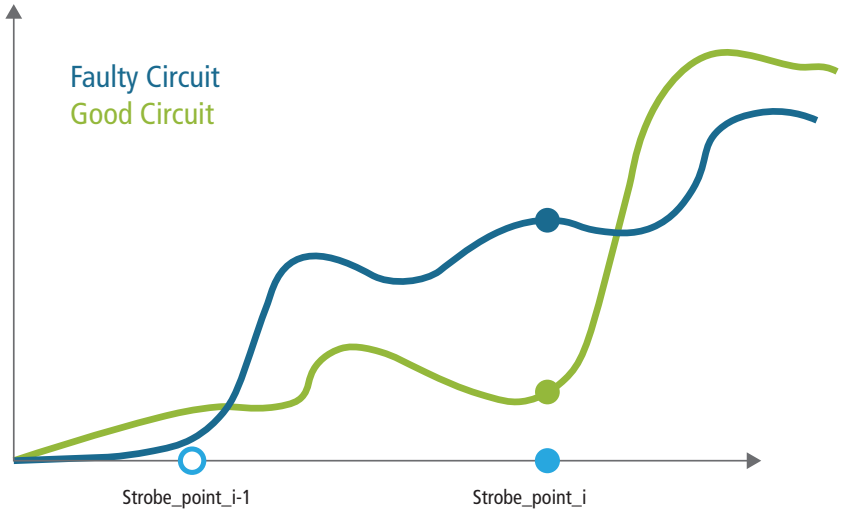

Figure 5: An example of DFA

TFA

The transient fault analysis (TFA) mode in Spectre APS incorporates several technologies for speeding up defect simulation. TFA takes advantage of the nature of test simulation to reduce simulation time. TFA provides several different modes for accelerating simulation. Table 1 compares the performance quality of results for DFA and different TFA methods. The results show that the simulation time can be significantly reduced by using TFA.

LDO 1151 total defects 1 strobe point	DFA	TFA			
		Method 1	Method 2	Method 3	Method 4
Speedup					
	1.0X	400X	80X	8.4X	4.1X
Defects Detected					
Detected	220	92	186	198	220
Defect Coverage					
Matched	100%	86.8%	91.5%	97.9%	100%

Table 1: Comparison of DFA vs. TFA results

Inside of the Virtuoso ADE Assembler, TFA can be used with optimized overall run time. After running the fastest TFA method, all the detected defects can be deleted from the fault list. The simulation can be re-run with the reduced fault list and the next fastest method. After the run, again all the detected defects can be eliminated, and the process repeated until all the defects are detected. The results for the LDO using this approach are shown in Table 2. The canonical simulation time compares the total DFA simulation time, 100%, to the run time for different TFA methods normalized to the DFA run time.

	DFA	TFA			
		Method 1	Method 2	Method 3	Method 4
Defects Detected					
Detected	220	92	186	198	220
Speedup from TFA					
Canonical Simulation Time	100%	0.25%	0.72%	11.84%	2.44%
Total Speed Up	1X	20X			

Table 2: Benefit of TFA

The Legato Reliability Solution provides designers different options for accelerating defect simulation time, giving them the opportunity to minimize the run time when exploring the overall testability of the design or high resolution when trying to get to signoff.

Post-Simulation Analysis

The last and most important step is to analyze the simulation results and extract useful information from them. What information would we like to extract?

- Overall test coverage, that is, the metric that we need to report to the end users of the product. Ideally, the test coverage is high enough to achieve the 0dppm target for the failure rate.
- The test coverage reported by test helps us to understand which tests are most effective and which tests are least effective.
- Reporting the test coverage by defect helps users understand which defects are not being found. This report is useful for debugging test issues and providing insight into how to increase the testability of the design.

Cadence enhanced the Virtuoso ADE Assembler to support analog defect simulation. As shown in Figure 6, the Assembler Fault Simulation mode is used to display the results of the defect simulation, including the overall coverage and the coverage by test.

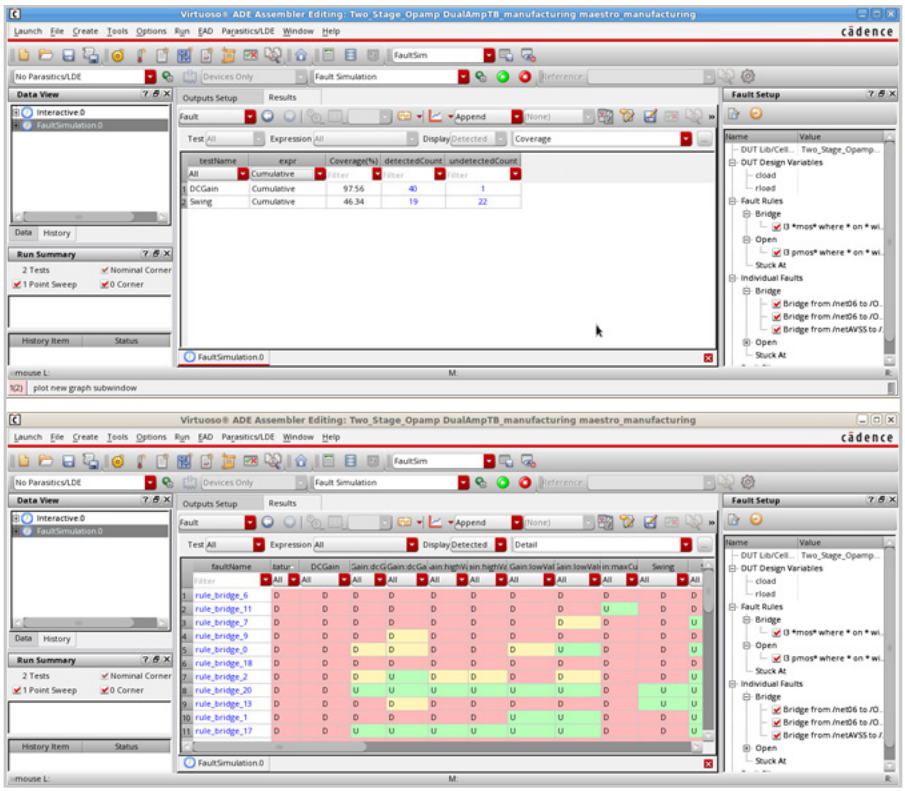

Figure 6: Virtuoso ADE Assembler fault simulation display

Coverage Summary

The Virtuoso ADE Assembler also provides the test coverage summary, shown in Figure 7, for all the tests and the corresponding measurements. The summary allows a designer to summarize the defect coverage for each test and measurement in a simple and easy-to-understand format.

testName	expr	Coverage(%)	detectedCount	undetectedCount
All	All			
DCGain	dcGain2	88.68	47	6
DCGain	lowValue	37.74	20	33
DCGain	problemDetected2	77.36	41	12
DCGain	lowValue2	83.02	44	9
DCGain	dcGain	41.51	22	31
DCGain	highValue	37.74	20	33
DCGain	highValue2	88.68	47	6
DCGain	problemDetected	24.53	13	40
Swing	RelativeSwingPercent	37.74	20	33
Swing	lowValue	16.98	9	44
Swing	problemDetected2	43.4	23	30
Swing	Swing2	30.19	16	37
Swing	Swing	37.74	20	33
Swing	lowValue2	13.21	7	46
Swing	highValue	26.42	14	39
Swing	highValue2	20.75	11	42
Swing	problemDetected	37.74	20	33

Figure 7: Test coverage report

Fault-Specific Data

The Virtuoso ADE Assembler also provides the results based on faults. The fault-based test report is shown in Figure 8. This format allows designers to identify faults that are not found by the test. The test results in green are tests that have passed, allowing the user to quickly identify which defects are not being found by the test program.

faultName	status	DCGain	DCGain:dcGain	DCGain:dcGain2	DCGain:
Filter	All	All	Filter	Filter	Filter
rule_bridge_9	D	D	25.0642n	5.47522u	-649
rule_bridge_8	U	D	998.404m	1.35342	199
rule_bridge_7	U	D	987.634m	-32.1785m	195
rule_bridge_6	U	D	1.00185	3.2767u	201
rule_bridge_5	U	D	993.192m	3.10392	197
rule_bridge_49	D	D	829.235m	2.35905	191
rule_bridge_48	U	D	991.952m	-3.27536m	197
rule_bridge_47	U	D	1.00253	17.0922u	201
rule_bridge_46	U	D	1.00514	38.3572m	202
rule_bridge_45	U	D	1.01242	1.29553	205
rule_bridge_44	U	D	1.00229	-3.28403m	201
rule_bridge_43	U	D	998.9m	625.999m	199
rule_bridge_42	D	D	-2.78816	3.15369	-528
rule_bridge_41	D	D	-26.8417n	1.44479n	544
rule_bridge_40	D	D	-2.13942m	5.48995u	-642
rule_bridge_4	D	D	3.37584u	5.52598u	-624
rule_bridge_39	D	D	793.387m	10.7462u	310
rule_bridge_38	D	D	-254.434u	987.193p	611
rule_bridge_37	U	U	983.844m	948.581m	193

Figure 8: Fault-based test report

Debugging the Fault Coverage

By just looking at list of faults, it is difficult to know where the fault is in the design hierarchy. Because the Legato Reliability Solution's analog defect simulation is based on the Virtuoso ADE Assembler, we can take advantage of cross-probing from the report back into the Virtuoso Schematic Editor. The location of the defect is highlighted in the block where the defect occurs, allowing designers to visualize why the defect is not found by the test and to make design changes to increase the observability of the defect.

Conclusion

While the analog and mixed-signal components are the leading source of test escapes that results in field failures, the lack of tools to analyze the test coverage during design has made it difficult for designers to address the issue. In this white paper we have explored the methodology for performing analog fault simulation of test coverage based on defect-oriented testing. Then we looked at how the Legato Reliability Solution can be used to calculate test coverage, and we demonstrated the feasibility of our solution on a practical design, enabled through an advanced fault simulation engine.

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