cadence®

Legato Memory Solution

Industry's first memory design, verification, and characterization solution

The Cadence® Legato™ Memory Solution provides a one-stop shop for all memory cell design, memory array and compiler verification, and memory characterization needs. The tight integration between the command-line cockpits and the simulators maximizes simulation throughput while maintaining accuracy for advanced-node memories.

Overview

The Legato Memory Solution consists of three cockpits. In the cell design cockpit, you can design the bitcell and perform Monte Carlo analysis. In the memory array and compiler verification cockpit, you can verify full memory arrays with high throughput across multiple PVT corners. In the memory characterization cockpit, you can create Liberty models of the memory to be used for SoC full-chip signoff (see Figure 1).

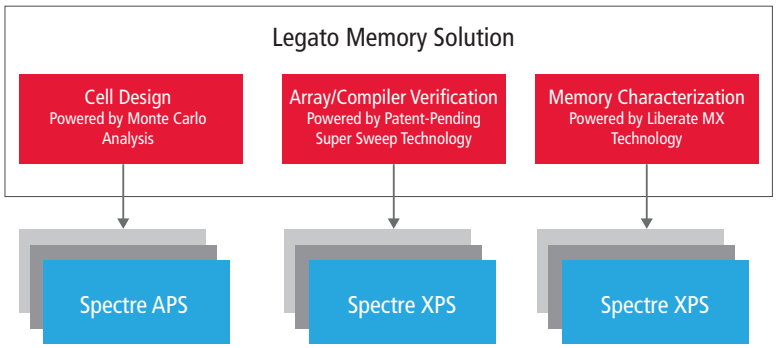

Figure 1: Legato Memory Solution overview

Key benefits

- Shared engines across design and characterization ensure consistency of results
- Better overall throughput through tight integration between different tools
- One-stop shop for all memory design, verification, and characterization needs

Cell Design Cockpit

In the cell design, you can invoke accurate, silicon-proven SPICE simulation with Monte Carlo analysis. The Cadence Spectre® Circuit Simulator or Spectre Accelerated Parallel Simulator (APS) can be used for simulation of small blocks in SRAM designs, such as bitcells and sense amps.

Key benefits

- Integrate with foundry-certified, silicon-proven, and fast-performance SPICE simulator
- Monte Carlo analysis for SRAM bitcells

Array and Compiler Verification Cockpit

In the array and compiler verification cockpit, you can verify timing margins and leakage across multiple PVT corners. Once the memory cell design is complete, you need to design and verify the whole memory instance. Its simulation engine uses the Spectre eXtensive Partitioning Simulator (XPS).

Leveraging the patent-pending Super Sweep technology (Figure 2) in the memory solution, you can maximize simulation throughput. This technology explores different steps in circuit simulation and optimizes them to provide you the best simulation performance. By sweeping through all PVT corners, it can group the appropriate suites of corners to maximize simulation throughput. A typical memory characterization run takes hundreds, if not thousands of simulations. The ability to provide simulation results quickly by leveraging the simulations that have been already completed is a major productivity enhancement for designers and verification engineers.

Furthermore, this approach works on Monte Carlo analysis. In Monte Carlo simulation, the entire netlist is simulated a large number (e.g., 1000-10000) of times. Each simulation is equally likely, and goes through similar simulation steps. In this case, the simulator outputs a large

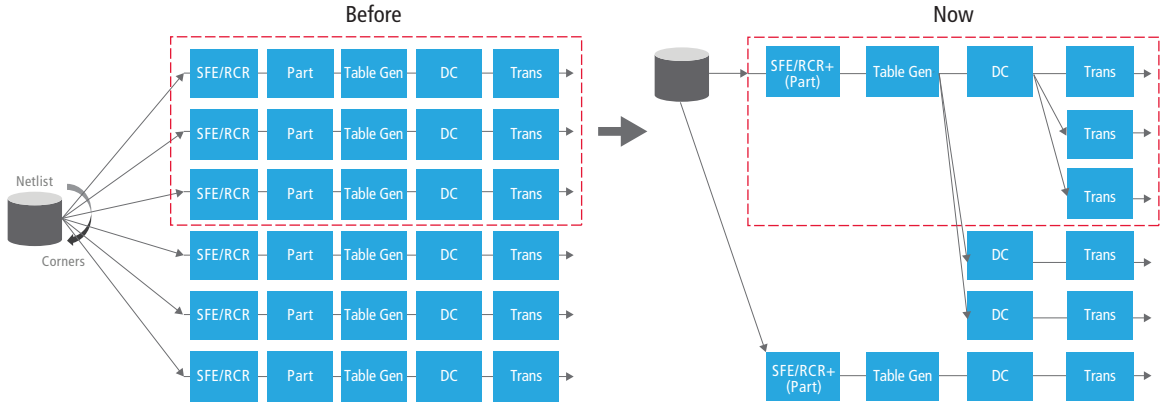

Figure 2: Patent-pending Super Sweep technology maximizes simulation throughput

number of separate and independent results, each representing a possibility. Instead of providing timing or power simulation results for each corner as the case in the multi-corner analysis, Monte Carlo analysis provides probability distributions, not single values. In this case, the simulator can provide probability distributions based on Monte Carlo analysis.

Key benefits

- Integrate with Spectre XPS, the high-performance and high-capacity pre-and post-layout simulator for memory design, delivering a significant reduction in simulation runtime compared to traditional FastSPICE simulators
- Patent-pending Super Sweep technology provides the best runtime performance for multiple PVT corners and Monte Carlo analysis

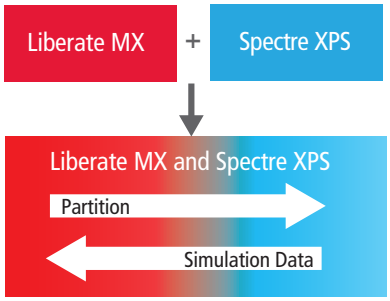

Figure 3: Tight integration between Liberate MX and Spectre XPS simulation

Memory Characterization Cockpit

In the memory characterization cockpit, you can generate timing and power Liberty models for your memory to be used in full-chip SoC verification. Leveraging a network of distributed CPUs and utilizing unique technology for optimizing characterization runtime, the Cadence Virtuoso® Liberate™ MX Memory Characterization Solution can easily and quickly generate accurate timing constraints and modeling of current source models for timing, power, and noise. During characterization, the enhanced Liberate MX solution partitions the netlist into small leaf-level pieces and uses Spectre circuit simulators for accurate simulation on each piece, as shown in Figure 3. Spectre XPS runs its most accurate mode at both the top and leaf levels to ensure accuracy. With the topology recognition and Super Sweep technology, Spectre XPS meets all simulation needs to provide accuracy and runtime at the same time. The tight integration between memory characterization and circuit simulation provides additional accuracy and performance improvements that can't be achieved by point tools.

Key benefits

- Provide accurate and fast memory characterization utilizing technologies specially designed for memories
- Enable full-chip SoC verification by accurately modeling memories in the CCS, NLDM, ECSM, timing, power, and noise formats
- Seamless integration with Spectre XPS to provide SPICE accuracy and fast runtime

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
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