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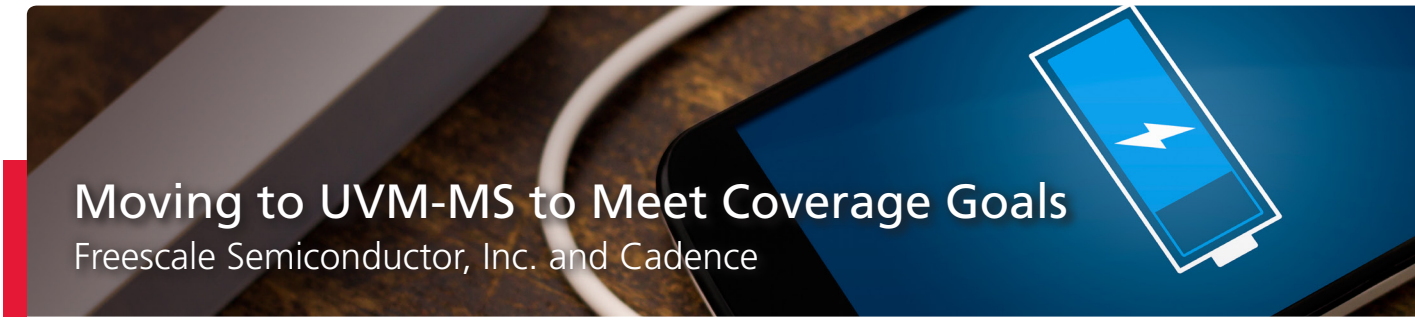

Moving to UVM-MS to Meet Coverage Goals

Freescale Semiconductor, Inc. and Cadence

About Freescale Semiconductor

Freescale Semiconductor, Inc. is a leader in embedded processing solutions for the automotive, consumer, industrial, and networking markets. The company's technologies include microcontrollers, microprocessors, sensors, and analog ICs. Headquartered in Austin, Texas, Freescale Semiconductor has design, R&D, manufacturing, and sales operations in more than 20 countries.

Key Challenges

At Freescale Semiconductor's analog and sensors division, the products managed mainly consist of analog components, despite the rapidly increasing use of digital logic in every new project. Most analog engineers have limited expertise in design verification languages. Still, their help in executing top-level verification of mixed-signal systems on chip (SoCs) is critical.

For analog engineers, testbenches are generally created with schematic entry and multiple configuration views and based on waveform inspection. However, advanced verification methodologies are typically digital centric—command-line driven and based on object-oriented languages such as SystemVerilog.

"Maintaining two top-level verification environments in order to tap into the expertise of both teams would be very impractical," noted Arthur Freitas, a design verification manager at Freescale Semiconductor. "We needed to find a more efficient way to verify our mixed-signal SoCs."

The Solution and Results

As a step forward, the Freescale Semiconductor verification team used a domain-specific language based on pre-processor macros and SystemVerilog APIs to create a digital-centric verification environment where analog engineers could perform self-checking top-level simulations. With Verilog configurations, users could select the design under test (DUT) abstraction required for each test case. Each test case is essentially a SystemVerilog file passed as a parameter to a simulation launching script.

Engineers can use a single hierarchical netlist for all simulations. After the netlist is created, all of the other simulation-related tasks can be performed outside the analog development environment using text-based files. The same pre-compiled netlist can be shared among all test cases.

Next, the verification team turned to the Universal Verification Methodology (UVM), integrating it into the design verification environment of their next-generation

Challenges

- Improve efficiency of top-level verification of mixed-signal SoCs
- Tap into expertise of digital and analog engineers for top-level verification

Cadence Solution

- Virtuoso Analog Design Environment
- Virtuoso AMS Designer Simulator
- SimVision Debug
- Incisive vManager solution

Lessons Learned

- To ensure backwards compatibility to the legacy directed-test environment, use compiler directives to constrain random stimulus
- When using a coverage- or metric-driven approach, simulation throughput is crucial, so it's important to collect enough metrics

Results

- Orders-of-magnitude faster top-level verification of mixed-signal SoCs using wreal configurations
- 2X more verification productivity for digital and analog engineers achieved through rapid simulation launch and re-invoke
- Better coverage and traceability with Incisive vManager solution
- Better bug detection using behavior wreal models verified against actual schematics

battery-monitoring IC. "To accomplish this, the UVM drivers had to use the same SystemVerilog APIs as the existing mixed-signal verification environment," noted Freitas. "To make this happen, the virtual interface references in the UVM drivers must command existing module-based APIs. Then, the UVM drivers can forward the transactions to the legacy module-based drivers."

Freescale Semiconductor used Cadence® Virtuoso® Analog Design Environment to implement its UVM/mixed-signal methodology. The environment provides all of the functions needed to fully explore, analyze, design, and verify analog and mixed-signal SoCs. The team also took advantage of the new unified netlister technology in Virtuoso Analog Design Environment, which speeds up the process of netlisting and elaborating a simulator snapshot with Cadence Virtuoso AMS Designer Simulator. They are using the Cadence SimVision Debug environment in Cadence Incisive® Enterprise Simulator to debug their mixed-signal designs. Using the Cadence Incisive vManager™ solution, the team has better coverage and traceability. Their resulting flow supports SystemVerilog, SystemVerilog-DC, SystemVerilog assertions, Verilog-AMS, VerilogHDL, and UVM.

"We've got orders-of-magnitude faster top-level verification of our mixed-signal SoCs using wreal configurations," noted Freitas. "And with our Virtuoso/Incisive platform, we can now reach mixed-signal verification closure more efficiently with higher quality results."

Added Freitas, "UVM brings the advantages of better coverage and better detection of hard-to-find bugs in a mixed-signal SoC. We can produce a substantial amount of test vectors with very little effort. Our digital designers can now easily port block-level tests developed in UVM to the top level—which was previously impossible. We can also integrate the UVM register layer at the IC top-level environment, which saves us quite a lot of development time in verifying register sequences."

Analog designers at Freescale Semiconductor have quickly adopted this new methodology. They can continue to develop directed tests using mixed-signal configurations in SPICE/behavior Verilog-AMS abstraction. Design verification engineers can complement top-level verification with UVM-powered constrained random stimulus using wreal configurations.

Lessons Learned

Cedric Fau, verification leader at Freescale Semiconductor, noted that backwards compatibility was important for the team. Because of this, they created a scenario file for each test. The UVM top module consistently runs the same uvm_test to call an external virtual task. As the actual test scenario, this external virtual task is implemented in a separate file.

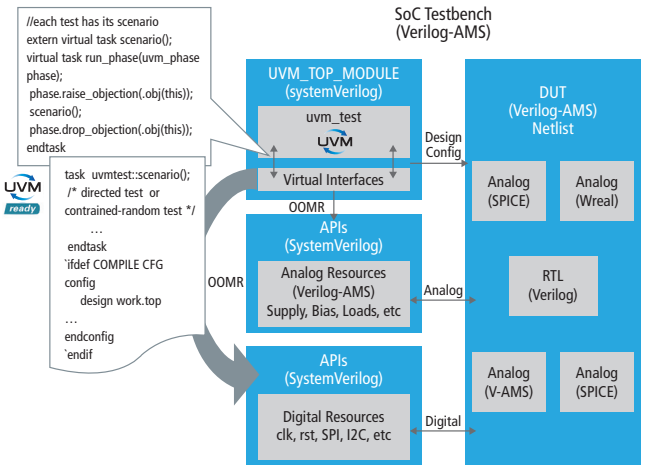

Figure 1: Freescale Semiconductor's UVM verification environment for mixed-signal SoCs

Now, engineers can execute existing legacy tests and also create new directed tests using the traditional methodology. Noted Fau, "The only thing that needs to be done is to constrain the UVM transactions generated with a generic sequence and map them to the legacy API macros."

Another lesson learned by the team is that, when using a coverage- or metric-driven approach, simulation throughput is crucial. So it's important to collect enough metrics. Modeling with real number models (RNM), i.e., Verilog-AMS wreal, or in SystemVerilog IEEE 1800-2012 is an effective way to increase the speed and effectiveness of simulations, noted Freitas.

Summary

By migrating from a module-based mixed-signal verification environment to UVM, Freescale Semiconductor gained a top-level mixed-signal verification framework that supports constrained-random verification. Concluded Freitas, "With the Cadence Virtuoso/Incisive platform-based environment, we now have a methodology that fosters 2X better productivity at the top level for both our analog and digital verification engineers. Our regression test suite not only gives us the confidence to perform fixes, both in the analog schematics and digital RTL, but also significantly reduces the verification effort for derivative products. We have overall better coverage and better detection of those hard-to-find bugs."

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