Taking the Fast Lane to Automotive Electronics Success
Thomas Wong, Director of Marketing, Automotive Segment, Design IP Group, Cadence

Introduction

Autonomous driving is a hot topic, and the enormous impact it will have on lifestyle and society at large cannot be fully comprehended at this time. As a result, everything associated with autonomous driving is receiving intense focus and analyzed for business impact and competitive advantage. Automotive ICs, particularly the complex systems on chips (SoCs) that perform the most complex functions, are at the very epicenter of that focus. They will play a critical role in enabling ubiquitous autonomous driving in the coming years. Analysts expect automotive semiconductors to be the fastest growing segment of the semiconductor industry, outpacing even the growth rate for smartphone electronics [1] (Figure 1).

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While electronics play a key role throughout modern vehicles, the major growth drivers can be segmented into two major application areas:

- Infotainment and the connected vehicle
- Advanced driver-assistance systems (ADAS) and advanced driving systems (ADS)

These new applications are not well-served by the traditional automotive ecosystem. The opportunities are more akin to the early stages of the smartphone market and are driving realignment within the ecosystem. This is creating huge opportunities for the companies that can adjust to the unique requirements of the automotive market. Helping our customers to meet those requirements rapidly and achieve success in the automotive market is a key focus area for Cadence, particularly in the area of design IP for automotive SoC developers.

Infotainment and the Connected Vehicle

Infotainment features can make or break a new car purchasing decision, so the rush is on to greatly improve the automotive user experience. People now expect their connected digital lifestyles to extend seamlessly into their vehicles with infotainment systems as intuitive to use as their smartphones. In addition, the design of infotainment systems has become staggeringly complex with consumers clamoring for the most innovative features. The key infotainment components include:

- Central vehicle control console
- HiFi audio system
- Navigation system
- Wi-Fi connectivity
- Bluetooth hub
- 4G and 5G telematics

Not only are the internal electronics supporting these components getting more complex, so too are the growing number of industry-standard interfaces that connect them (Figure 2). Both the internal and external SoC interfaces require a variety of design IP components. Acquiring high-quality commercial design IP speeds along the laborious task of SoC integration and provides an opportunity for SoC developers to achieve the coveted, and profitable, first-to-market status.
The Cadence® design IP portfolio spans the range of data communication and memory interfaces found in infotainment systems. For example, the IP solutions provide a PHY and controller for cameras connected via MIPI® standards, charging connectors through USB, updating maps through an SD interface, and driving high-definition display connectivity. Internal to the components, our widely used LPDDR PHY and controllers keep data streaming throughout the system.

ADAS and ADS

The ADAS and ADS segment, essential for enhancing the driver experience and overall safety, is one of the fastest growing segments within the automotive semiconductor space. Autonomous driving is leading to major disruptions in the automotive industry because ADAS applications require a performance level that goes far beyond popular microcontrollers. A new class of high-performance SoC is needed to collect and synthesize data from multiple sensors—a function known as sensor fusion (Figure 3).

In addition, ADAS SoCs enable vehicles to become “aware” of their surroundings. High-definition digital maps and cloud-based services are leveraged by the intelligent systems to provide precise and partially redundant information to further enhance the driver’s awareness and ability to safely control the car in real time, and in all driving and environmental conditions.

While many of the same interfaces utilized in infotainment systems are also used in ADAS systems, one interface of particular importance is Gigabit Ethernet with TSN—a fast and low-latency interface for time sensitive networking. The expanded use of this interface will greatly simplify vehicle cabling and reduce cost while increasing reliability and serviceability. Cadence was an early leader in IP for Ethernet with TSN and continues to enhance our offerings as the specifications behind it evolve and expand.

In addition to interface IP, a critical building block of ADAS SoCs is processor IP. Unlike standard processors like those in smartphones and laptops that are optimized for system control, the processors for ADAS must meet the computational demands of artificial intelligence (AI) and machine learning (ML). Processors of this type require the ability to perform staggering numbers of mathematical calculations. While cloud datacenters tap fast but power-hungry graphical processor units (GPUs) for AI and ML, edge devices including cars are best served by digital signal processors (DSPs) that can crank out trillions of multiply-accumulate (MAC) operations on a trickle of energy consumption.

Looking at both interface and processor IP, the key ADAS requirements include:

- **High compute performance:** 1TMAC/sec in a single square millimeter of silicon area to support compute-intensive algorithms and delivering an optimal SoC performance, power, and area ratio
- **High network bandwidth:** 1Gbit/s or more to support a low-latency transmission of high video/image resolution or control data
- **High memory bandwidth:** 3Gbit/s data-rate interfaces and sufficient memory capacity to store and access intermediate results generated by highly complex AI/ML algorithms
- **Low power consumption:** 9W power consumption or less for typical ADAS applications

The Cadence Tensilica® line of AI/ML, vision, audio, and communication processors, combined with the portfolio of interface IP is an ideal combination for meeting these challenging requirements.

— Masahiro Suzuki, Vice President of the Automotive Solutions Business Unit, Renesas Electronics Corporation

"Renesas has been the world leader in providing automotive computing SoCs for a long time. We are seeing increased adoption of advanced MCUs in automobiles to accelerate autonomous driving, connected cars, and electric vehicles. To address these trends in a timely manner, we have been working with Cadence on the development of physical IP using cutting-edge process nodes. Cadence has delivered advanced solutions for LPDDR4/X PHY that support the highest LPDDR4 memory speed available in the market."

Figure 2: Standardized electronics interfaces in automobiles

Figure 3: ADAS sensor fusion
**Functional Safety**

While it’s clear that advanced automotive SoCs have share many requirements with smartphone or cloud datacenter applications, there is one preeminent and extremely challenging requirement for automotive electronics: designing for functional safety.

Universally accepted as fundamental to automotive electronics design, and codified in ISO 26262, designing for functional safety can be understood as analyzing for, and incorporating countermeasures against, potential weaknesses in design—aspects of an SoC design that make it susceptible to mission failure from transient errors that can occur during normal vehicle operation. Such failures in ADAS applications could be catastrophic to the vehicle occupants, and would shatter consumer trust just as the technology is ramping up.

While the electronics industry has long taken measures to address manufacturing quality, the concept of designing for functional safety is still novel in consumer electronics circles and requires IP and SoC developers to adopt a disciplined design methodology, a robust set of analysis tools, and a dedicated organization culture.

As defined in ISO 26262, the Cadence automotive IP portfolio is designed to be ASIL-B ready. Our development teams undergo rigorous training in ISO 26262 requirements and are enabled by the company’s industry-leading functional safety analysis tools. Informed by learnings from our expert partners and leading-edge customers, we enable mainstream SoC developers to reduce their risk in automotive SoC development with IP designed from the ground up for functional safety and support with extensive safety manuals and other documentation.

**Semiconductor Technology**

The earliest chips designed to support automotive applications were designed more than 40 years ago, an eternity in the technology business. These chips were developed by semiconductor integrated device manufacturers (IDMs) because they could control every step of the design, manufacturing, testing, and qualification. This approach was useful for electric control units (ECUs), for engine and transmission control, for instance, and still makes sense today for those applications.

But as electronic components have evolved beyond the engine compartment, so too have the semiconductor processes needed to support them. While some in-vehicle networking can be implemented with acceptable performance in 40nm semiconductor technology, and mainstream infotainment SoCs need at a minimum the performance obtainable from 28nm technology, ADAS systems require a performance level only obtainable in 16nm technology, with future requirements clearly trending on to 10/7nm.

To support these advanced applications, Cadence offers a comprehensive automotive IP portfolio in 16nm FinFET technology (Table 1). This broad IP portfolio enables a host of applications ranging from in-vehicle infotainment, in-cabin electronics, vision subsystems, digital noise reduction, and ADAS subsystems. To support cost-effective automotive SoC designs, Cadence IP is area- and power-optimized for the AEC-Q100 Grade 2 temperature range, eliminating the need to carry Grade 1 power and area penalties into cost-sensitive automotive SoC designs.

Cadence has a comprehensive automotive IP portfolio in 16nm FinFET technology. This portfolio enables a host of applications ranging from in-vehicle infotainment, in-cabin electronics, vision subsystems, digital noise reduction, and ADAS subsystems. The portfolio incorporates the key IP needed to implement advanced infotainment and ADAS SoCs and includes the Cadence flagship 4266-speed grade LPDDR4/4X DDR PHY and controllers and PCI Express® (PCIe®) 4.0/3.0 PHY and controllers. This is complemented by subsystems supporting MIPI® D-PHY™, USB 3.1/USB 2.0, DisplayPort, Octal SPI/QSPI, UFS, and Gigabit Ethernet with TSN.

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“Cadence has quickly adapted its IP portfolio to support automotive applications for our 16FFC process, enabling accelerated design-ins with major automotive suppliers. Our ongoing collaboration with Cadence has resulted in a robust, comprehensive set of IP that enables today’s complex automotive designs for ADAS applications and infotainment systems.”

Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division

**Unique Strengths**

Cadence brings to bear a unique combination of strengths to assist our customers with the challenge of automotive SoC design. As touched on above, these strengths include:

- Comprehensive interface IP portfolio for the high-growth infotainment and ADAS applications
- Industry-leading Tensilica DSP IP addressing AI/ML, vision, audio, and communication needs
- Extensive functional safety experience, use of the most advanced analysis tools, and strong design-for-safety culture
- Broad support for the industry-leading 16nm semiconductor process with future growth to even smaller geometries
- A unique collaborative approach to SoC enablement
This last point is what our customers most appreciate in having Cadence as their automotive IP partner. Cadence understands that collaboration and flexibility are key to a successful partnership, and that we’re not successful unless our customer is successful.

So, we invite you to select Cadence as your IP partner, and take the fast lane to automotive electronics success!

References