OVERVIEW

CADENCE VERIFICATION IP (VIP) INTEGRATION SERVICE

Cadence® Verification IP (VIP) Integration Service allows you to quickly utilize Cadence Incisive® Universal Verification Components (UVCs) to maximize chip- and system-level verification productivity. Leveraging verification IP in the form of UVCs jumpstarts your verification process, helping you achieve metrics and coverage in days. The program delivers onsite consulting, development services, and Incisive verification technologies along with written recommendations for next steps.

AUTOMATING SYSTEM-LEVEL TESTBENCHES WITH UVCS

Incisive Universal Verification Components (UVCs) have proven their value for automating block-level testbenches over many years. However, system-level testing is still performed using less powerful directed test techniques. Now, combining the vast portfolio of Incisive UVCs with the ability to reuse Incisive UVCs at both chip and system levels—without any code change—there is a compelling reason to consider UVCs as the cornerstone of your system-level verification environment. Incisive UVCs provide automated test generation, automated planning and management, and compliance management utilities to ensure protocol correctness. This highly automated environment finds bugs faster with constrained-random test generation, identifies functional verification holes more easily, and reduces the burden of test management—all while maximizing productivity with proven verification component reuse.

LEVERAGING CADENCE VERIFICATION EXPERTISE

The challenge in adopting any new methodology is putting something together for the first time and then proving the value of the change. Typically there isn't enough time, deep methodology knowledge, or personnel to do a proper job. Cadence VIP Integration Service eliminates those risks with a pre-packaged service that will deliver your first test in days and a fully functional metric-driven environment in mere weeks. We will teach you how to build the environment, how to automatically generate, direct, measure, and track verification progress, and optionally provide protocol expertise for rapid ramp and integration of an integration interface. Cadence verification experts leave you with a comprehensive environment that integrates your UVCs and puts you on the path to final chip or system-level validation. At the end of the engagement, Cadence provides a report indicating what bugs were identified, how to proceed, and which tools or overall methodology enhancements might be needed.

BENEFITS

- Delivers a full-featured functional system-level testbench in mere weeks, saving time and increasing productivity
- Reduces risk by leveraging a proven and pre-engineered program
- Uses a metric-based approach for increased quality, visibility, and predictability
- Improves productivity by using state-of-the-art functional verification techniques

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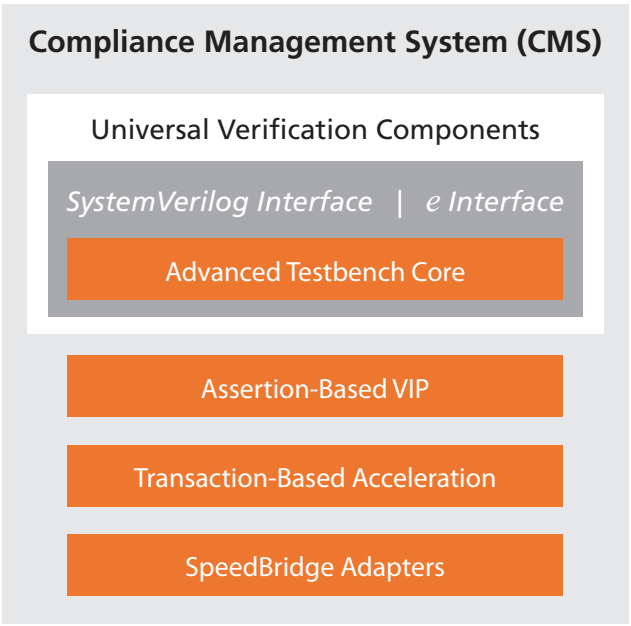

Figure 1: Comprehensive Cadence Verification IP Integration Service

METRIC-DRIVEN VERIFICATION

The key to successful coverage-driven verification is not just constrained-random test generation. While this helps to reduce direct test writing and management, it does not show you how to plan and manage highly effective verification scenarios. Most experts agree that a metric-based coverage-driven verification solution is the best way to maximize bug identification while minimizing time. Studies have proven that combining constrained-random testbench generation with a focus on specific functions that need to be verified (coverage points) keeps you focused and gets you to functional verification closure faster than with any other known technique. Forget the manual spreadsheet tracking approach; use the automation provided in the Incisive platform to focus on those new tests that are needed, rather than re-running tests that are duplicate and do not advance functional closure. This Cadence metric-driven verification solution embeds years of experience and gets you from planning to closure quickly.

ENGAGEMENT PROCESS

Cadence VIP Integration Service begins with the identification of a specific project. We will review your current testbench methodology and DUT to identify functional coverage points and the required UVCs. For existing environments that do not include functional coverage, we will discuss your verification goals and together write an executable verification plan that determines coverage points (which features you would like to focus on). Cadence will provide a written implementation plan for the project and work with you to develop and enhance your verification strategy. Additionally, Cadence can provide a protocol expert to advise you on protocol specifics, consult with you on how to plan integration verification, and work with you to build a working environment to exercise those tests.

DELIVERABLES

- Analysis of the chip or system verification with delivery of an implementation plan
- Full-featured and functional integrated metric-driven environment consisting of multiple Incisive UVCs and Incisive Enterprise Manager
- Optional protocol consulting and implementation by protocol experts
- Optional protocol compliance management verification
- Final report recommendations for improving verification coverage
- Onsite consulting

For more information contact Cadence sales at:

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