

# Cadence VULCAN - Virtuoso Utility for Library Creation and Analysis

For Cadence Virtuoso, Encounter, and Incisive Users

The Cadence® Virtuoso® Utility for Library Creation and Analysis (VULCAN) solution provides an automated approach to accurately capture both the electrical and the physical characteristics of shared mixed-signal design library IP through the use of a standard interface format and an associated use model. VULCAN is integrated with the Virtuoso platform, so it can process data from the Cadence Incisive® and Cadence Encounter® platforms. With this solution, you can accurately reuse external IP.

## Overview

In an AMS design, you need to accurately re-use external IP using the same design manufacturing process. Usually the design environment used to create the targeted design and the IP itself might be quite different (e.g. different tools suite, different process design kits (PDKs), different methodologies, etc).

The challenge in importing/exporting third-party IP is to accurately capture both the electrical and the physical characteristics of an IP within its own PDK for a different target AMS design environment. Ultimately, what you strive to do is to facilitate consistent data import/export exchange for a smooth implementation and verification process.

Provided as a Virtual Integrated Computer-Aided Design (VCAD) Productivity Package, the Cadence Virtuoso Utility for Library Creation and Analysis (VULCAN) solution achieves this goal by providing an automated approach to unify and qualify shared mixed-signal design library data through the use of a standard interface format and an associated use model.

## IP Integration Challenges

As product development windows become smaller and smaller, you're required to perform more and more block re-use instead of designing the entire integrated circuit from the ground up. There are different types of re-use:

- Acquiring a third-party qualified IP designed on the same design manufacturing process as your product
- Migrating an existing block from another process node and enhancing it to fit the current design requirements. In this case, you can expect electrical and topology changes.
- Providing a re-usable IP to an external partner with a potentially different design environment

The challenge in importing/exporting third-party IP is to accurately capture both the electrical and the physical characteristics of an IP within its own PDK for a different target AMS design environment.

## Benefits

The VULCAN environment provides a graphical utility that captures an import/export methodology. This aligns the third-party IP with the current design PDK and ensures that all tools of the AMS design are enabled with this IP. The methodology involves both a thorough data preparation and a set of validation stages. VULCAN is integrated within the Virtuoso platform for processing data from both the Cadence Incisive and Cadence Encounter platforms.

For IP protection, VULCAN also provides a way to export encrypted CDL/SPICE/Cadence Spectre® and GDSII files. This will secure design hierarchy, naming conventions, and netlist content.

VULCAN is a general-purpose infrastructure that creates a high-quality library structure based on standard file description. A Virtuoso SKILL-based software, VULCAN automates the import or creation of various representations of the IP. VULCAN not only creates the views but also uses various other Cadence tools to check

the validity and the consistency of created views with reference input data, and also between the created views themselves.

Figure 1 shows the VULCAN IP import user interface.

**Features**

**Import flow**

Starting points for an IP import are the standard interfaces - the design should have at least a SPICE (or SPICE-like) netlist for circuit simulation and a GDSII file for physical design. Based on these two description files, the VULCAN library processor reconstructs all necessary views for an AMS design environment based on the Virtuoso environment, like:

- Symbol, which defines the IP pin interface to the design in schematic entry
- Hierarchical schematic view, which defines the IP device network
- Layout view, which is necessary for final chip sign-off assembly
- Abstract view, which is necessary during chip floorplanning and automatic routing (when applicable)
- Extracted view formats (Virtuoso OA extracted view, DSPF, SPEF, EPS Power Grid database), which is necessary for post-layout simulation

If the IP is also intended to be used in a digital place-and-route flow, the following views are also necessary:

- ETS noise characterization views on when at input we have a proper timing .lib description of the IP
- EPS power views

VULCAN also generates CDL, SPICE, and Spectre netlists to be used in various design steps where the IP is treated as a black box (simulation and LVS).

Figure 2 depicts the import flow details.

**Export flow**

IP export uses the same infrastructure as that of IP import. The same data sets are generated and qualified. The starting point for the IP export is a DFII hierarchical design with the following views:

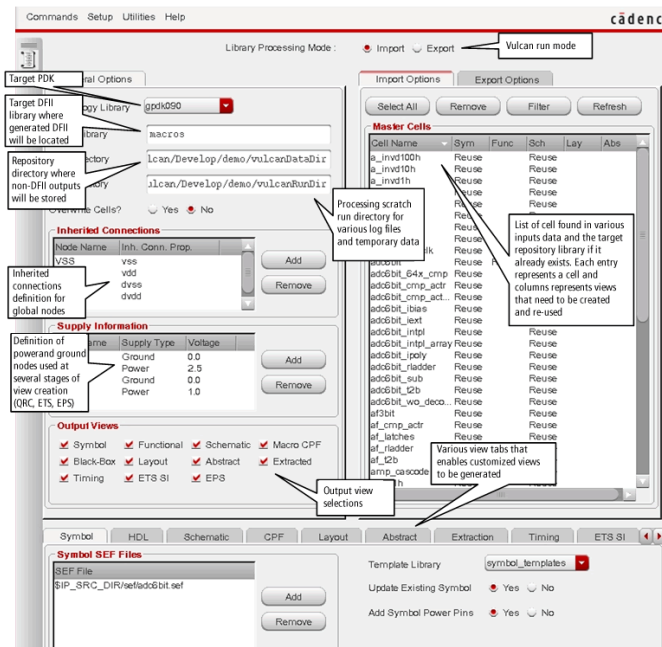


Figure 1. VULCAN IP import user interface

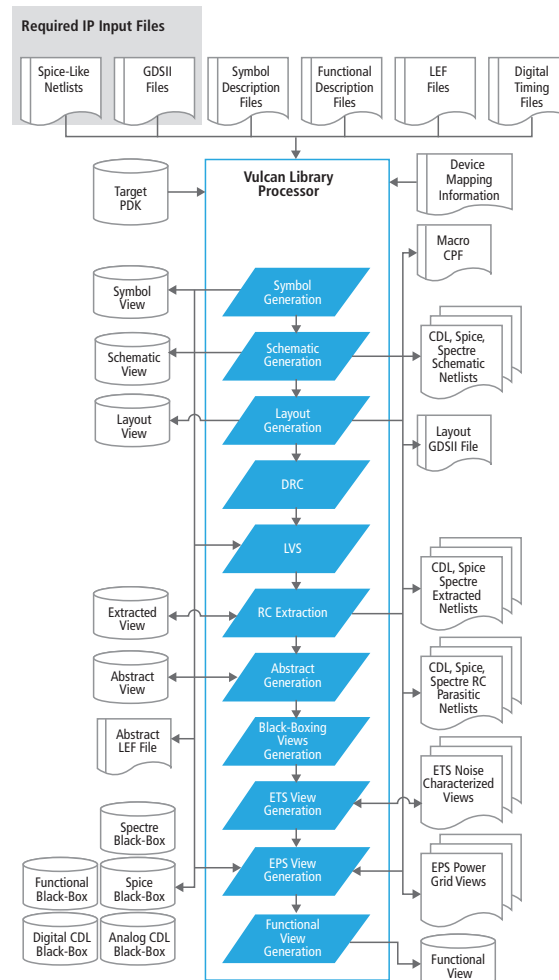


Figure 2. Import flow details

- **Symbol:** It is used as the reference view for deriving the I/O interface of the IP
- **Schematic:** It is used as the connectivity reference. It is imperative for this view to be checked and saved without errors in VSE. Otherwise, it could not be netlisted.
- **Layout:** It is used as the physical footprint of the IP

After the export process, the following non-DFII views will be generated for digital place-and-route integration:

- Hierarchical CDL netlist - device model name complies with external LVS requirements
- GDSII file of the IP - layer mapping complies with external physical verification requirements (DRC, LVS)
- Hierarchical SPICE netlist - device model complies with external SPICE simulation requirements
- Flat layout extracted Spectre and SPICE netlists with and without RC parasitics - device model complies with external Spectre and SPICE simulation requirements
- Macro library exchange format (LEF) with antenna information required for place-and-route chip assembly
- CeltIC crosstalk noise characterization views of specified temperatures and model corners
- VoltageStorm Static (VSPE) static power views for electromigration (EM) and IR drop analysis

Figure 3 depicts the export flow details.

VULCAN provides a way to encrypt the data if the IP provider wants to protect their IP from being reverse engineered. Figure 4 is an example of an obscured CDL netlist.

### Required Design Environment

The following infrastructure is required for a successful VULCAN IP import/export with all possible views:

#### Cadence software stream

- Virtuoso 6.1
- PVE stream

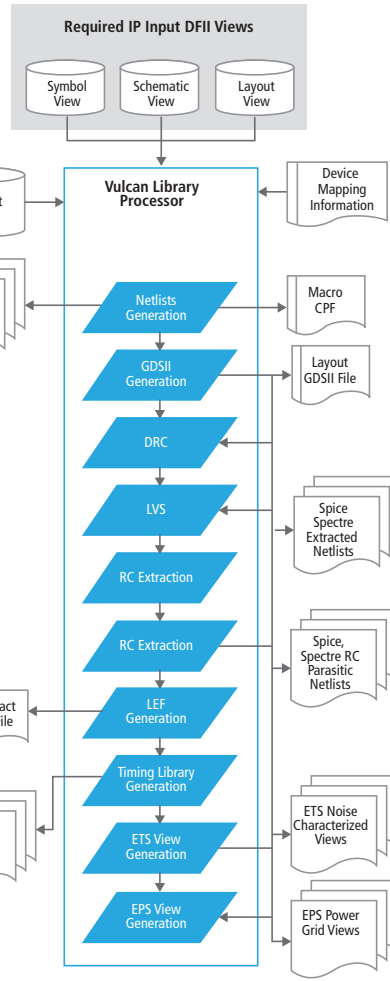


Figure 3. Export flow details

```
** Model : lqtTjnY
Encrypted model name      Model connectivity is
                          preserved
SUBCKT lqtTjnY m1 Q ON RN inh_DVDD inh_TVSS
M1a0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1b0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1c0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1d0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1e0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1f0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1g0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1h0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1i0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1j0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1k0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1l0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1m0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1n0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1o0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1p0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1q0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1r0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1s0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1t0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1u0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1v0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1w0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1x0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1y0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
M1z0d007Y H3bE9w2a ba3F20XK bVfEe0D inh_DVSS rmos2v L=2 8e-07 m=1 w=5 6e-07
.ENDS
```

Figure 4. Obscured CDL netlist

- Incise platform, required for functional view creation and validation
- ETS noise views, required for digital integration in EDI
- EPS static power grid views, required for digital integration in EDI

### PDK requirements

- Support CDL netlisting as a basis for GDSII-based physical verification
- Support of PVE for physical verification for both DFII- and GDSII-based flow
- Support QRC for RC extraction with support for cap\_ground\_layer feature
- Support of tablegen models by EPS static power grid views generation
- Support of XTC and RCgen extraction for EPS static power grid views generation
- Availability of technology LEF required for EPS static power grid views generation
- Device Spectre models must be provided

- Device SPICE models must be provided. Otherwise, EPS power grid views generation will fail for designs containing non-MOS devices
- Support of abstract generation

#### VULCAN set-up requirements

- Stream layer file extracted from the PDK is necessary for GDSII manipulation. This file uses the same format as the usual XSTREAM layer mapping file
- Creation of a base abstract generation options file
- Creation of device mapping file requires SPICE-like netlist import and various netlist translation operations during the import phase
- Creation of “special” PVS set-up file required for VULCAN infrastructure

#### Supported Design Environment

- Fully integrated within Virtuoso platform for processing Virtuoso, Incisive, and Encounter data
- Tools: IC 6.1.5/IC6.1.6, PVE 12.1, EDI 11.1/13.1, Incisive 12.1, ETS 12.1, EPS 12.1

#### VCAD Productivity Packages

VCAD Productivity Packages are a set of pre-packaged generic core solutions that increase design system productivity. Productivity Packages are available within services contracts, which include the package integration and maintenance of the customized solution. Cadence VCAD services targets the development, implementation, and ongoing improvement and maintenance of productive design systems to ensure short time to market and silicon success.

VULCAN is available through Cadence VCAD Services. For more information, please contact:

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