The Cadence® Analog/Mixed-Signal (AMS) Design Methodology employs advanced Cadence Virtuoso® custom design technologies and leverages silicon-accurate design flows to help design teams create differentiated silicon faster and with less risk. It delivers verified and packaged methodologies demonstrated on a real-world mixed-signal design. The Cadence AMS Design Methodology combines the best of top-down (behavioral and mixed-level approaches) with bottom-up (transistor-level design and abstraction) design techniques to achieve predictable, high-quality results for complex mixed-signal designs.

AMS DESIGN METHODOLOGY

The Cadence AMS Design Methodology delivers an extensive design and data flow guide, from design specification through design manufacturing, across the different functions of a design team. It is based on executable design tasks and recommended use models for fast, silicon-accurate mixed-signal design that ensures first-pass silicon success. The AMS Design Methodology addresses the analog-driven mixed-signal design process front to back by executing well-defined flows that demonstrate a meet-in-the-middle approach, in which all design flows are running in parallel to minimize design iterations, maximize project resource utilization, and enhance design quality.

The AMS Design Methodology addresses the entire design process and comprises five major flows:

1. Design environment and infrastructure
2. Top-down functional verification
3. AMS IP block creation and reuse
4. AMS IP export and integration
5. Top-down physical design
The five flows are further divided into modules of logically related design tasks, which are illustrated and documented with in-context scenarios. The different scenarios are demonstrated on a silicon-implemented and verified real-life design, namely an Ethernet physical layer macro (PHY) and a sigma-delta fractional-N PLL frequency synthesizer macro for WLAN applications. The Ethernet PHY contains 20k analog devices and 30k digital gates including typical analog, digital, and mixed-signal blocks such as flash ADC, VGA, equalizer, and clock recovery circuit. The fractional-N PLL is a 2.4GHz synthesizer that contains 20k devices and includes a 5GHz LC VCO, a high-speed divider, on-chip regulators, and a calibration mechanism for loop filtering and VCO.

Both Ethernet PHY and frac-N PLL are implemented on a 90nm generic process design kit (GPDK), which has virtually all the aspects of an actual design kit. The design blocks have all the necessary views for complete design, including symbols, schematics, constraints, behavioral models, abstracts, layout, and extracted views, as well as configurations, testbenches, and simulation states. A design team can use the reference design as a basis to enter a new design domain, understand a wide range of new Virtuoso technologies, acquire new methodologies, and map selected elements onto their own design environment.
FEATURES

DESIGN ENVIRONMENT AND INFRASTRUCTURE

Any design process takes place in a certain environment including different projects, CAD tools, process design kits (PDKs), and users on different hardware platforms and operating systems. It is very important to create a consistent design environment to ensure the quality of the design and the credibility of the results.

This part of the Cadence AMS Design Methodology gives the foundation to set up a design environment using tested and proved methods and technologies, including incremental tool access, project directory structure, how to set up and control PDKs, and how to automate project and flow setup using the Design Environment and Configuration Manager.

The data exchange between the design house and the foundry is explained, detailing required datasets from the foundry and how to qualify them against the defined AMS flows. Special attention is given to the PDK—how to automatically check its content using the Data Surveyor and how to use the Incremental Technology Database (ITDB) to customize and enhance the PDK.

TOP-DOWN FUNCTIONAL VERIFICATION

A comprehensive functional verification flow is presented, spanning all levels of abstraction and all design stages, from planning to post-layout device-level signoff verification. First, an introduction to the concept of design partitioning and simulation planning is given. Next, behavioral modeling guidelines and testbench strategies are presented.

A consistent testbench structure is used over all later stages of verification, starting with concept validation using behavioral model representation in AMS simulation, and system validation using Simulink/AMS co-simulation. Next is performance validation using mixed-level-transistor plus behavioral-level simulation on Virtuoso AMS Designer Simulator with SDF backannotated to the digital part.

Finally, a post-layout and signoff verification is prepared to include both analog extracted parasitics and SDF backannotation for the most accurate timing estimation using Virtuoso AMS-Ultra Simulator. An IDDQ analysis is performed using full extracted transistor-level DC simulation with the Virtuoso UltraSim Full-Chip Simulator along with top-level EM IR drop analysis.
AMS IP BLOCK CREATION AND REUSE

A thorough approach to creation of both analog and digital blocks is presented using productivity-oriented Virtuoso technology. The constraints concept and management is used to amend the schematic with the required information to automatically create its layout. Furthermore, constraints can be inferred from pre-defined circuit structures using the Circuit Prospector Assistant.

New layout techniques like design-rule–driven (DRD), module generator (Modgen), and constraint-driven editing are shown in action through a dedicated assisted layout module. A new approach to simulation is shown through the specification-oriented simulation platform (Virtuoso Analog Design Environment) with its numerous productivity enhancement features including simulation history, check points manager, parameterization flow, design specifications, and parasitic estimation flow. The high-capacity Virtuoso Analog Design Environment optimization engine is used for local and global optimization on the block level, over corners, and as a yield optimizer with Monte Carlo and sensitivity analyses.

AMS IP EXPORT AND INTEGRATION

The IP flow is a comprehensive guide for analog and digital IP handling, from top-level integration to extensive characterization and packaging. On the exporting side, a complete step-by-step scenario of characterizing and modeling an analog IP in Verilog®-AMS is presented, taking an N-bit flash ADC as an example. Automated testbench extraction is discussed; generic behavioral model planning, coding, and debugging is illustrated. The model includes advanced features like noise, aperture time, INL, and DNL parameters. The layout abstract is generated using the Virtuoso Abstract Generator. The timing information (.lib) file for top-level digital integration is generated using Virtuoso Spectre® MDL language and verified by importing to the Cadence Encounter® platform. Finally, packaging of all generated views for publishing is discussed and implemented using Vulcan technology.

Figure 6: AMS IP block creation and reuse

Later, Virtuoso Layout Optimizer is used to boost the yield on the back end. A tutorial introduction to analog-driven digital implementation using the Virtuoso Digital Implementation Option shows a typical digital layout flow including planning, prototyping, placement, routing, timing optimization, clock tree synthesis, SDF generation, parasitic extraction, and parasitic closure.

Figure 7: AMS IP export and integration
On the importing and integration side, feasibility of IP integration employing multi-technology simulation (MTS) is exemplified, followed by actual import using Vulcan technology. Legacy cdb file import into the Virtuoso OpenAccess (OA) database is shown. Importing of digital IP in an analog context is also presented.

**TOP-DOWN PHYSICAL DESIGN**

The physical design flow introduces a true top-down approach to chip layout using state-of-the-art Virtuoso technologies. Special emphasis is given to early floorplanning to get information about the critical parasitics to feed back to the verification flow. This is possible through a Virtuoso Floorplanner, a Physical Hierarchy Configurator, and an Abstract Generator, along with several floorplanning techniques like connectivity analysis, area estimation, pushdown block shaping, and pin optimization. The flow is illustrated on the PLL.

The analog-oriented physical assembly and routing is described using both Virtuosos Chip Assembly Router and Virtuoso Space-Based Router, both accepting design constraints. The flow is demonstrated by top-level routing of the Ethernet PHY and the PLL macro using advanced analog routing techniques like critical signal, differential signal, shielded signal, bundle, and supply routing. After routing, chip finishing is applied, including metal density and antenna checks, metal filling, and guard rings.

The assembled layout is then verified using Cadence Assura® verification technology with dedicated scenarios for Design Rule Checking (DRC), Layout Versus Schematic (LVS) checking, and Parasitic Extraction (RCX) applied to the Ethernet PHY. A comprehensive guide to practical Assura features like flat and hierarchical, black-box or selected area checking, different netlisting, and extracted parasitic formats is illustrated.

**EXECUTABLE SCENARIOS**

**DESIGN ENVIRONMENT AND INFRASTRUCTURE FLOW**
- AMS design flow overview
- Foundry enablement
- Project environment setup
- Automated project setup with the Design Environment and Configuration Manager
- Reference Data Surveyor
- ITDB implementation

**TOP-DOWN FUNCTIONAL VERIFICATION FLOW**
- Design partitioning and simulation planning
- Concept validation
- AMS/Simulink co-simulation
- AMS functional verification
- Signoff functional verification
- IDDQ simulation
- EM IR drop analysis with DSPF stitching

**AMS IP BLOCK CREATION AND REUSE FLOW**
- Constraint-driven analog block creation
- Analog block design simulation
- Analog block design optimization
- Interactive assisted analog layout
- Electrical yield optimization
- Layout yield optimization with Virtuoso Layout Optimizer
- Digital block implementation

**AMS IP EXPORT AND INTEGRATION FLOW**
- Analog IP characterization, front end
- Analog IP characterization, back end
- IP import feasibility study using MTS
- IP Import using Vulcan methodology
- IP import for Virtuoso methodology
• Virtuoso integration of digital IP
• Digital IP characterization
• IP packaging for publishing and reuse

TOP-DOWN PHYSICAL DESIGN FLOW
• Hierarchical floorplanning
• Top-level assembly with Virtuoso Chip Assembly Router
• Top-level assembly with Virtuoso Space-Based Router
• Chip finishing
• Physical verification Assura DRC
• Physical verification with Assura LVS
• Parasitic extraction with Assura RCX

PRODUCT INTEGRATION
• Virtuoso Multi-Mode Simulation
• Virtuoso Spectre Circuit Simulator
• Virtuoso AMS Designer Simulator
• Virtuoso UltraSim Full-Chip Simulator
• Virtuoso Analog Design Environment (ADE)
• Virtuoso Schematic Editor
• Virtuoso Layout Suite
• Virtuoso Layout Migrate
• Virtuoso Analog VoltageStorm Option
• Virtuoso Analog ElectronStorm Option
• Assura Design Rule Checker (DRC)
• Assura Layout vs. Schematic (LVS) Verifier
• Assura Parasitic Extraction (RCX)
• SoC Encounter™ RTL-to-GDSII System