OUTLINE

- Short-Reach Optical Interconnect Roadmap
  - Cu-to-Optical Transition Roadmap
- 50G NRZ Silicon Photonics Platform
  - Passive Devices
  - Modulators
  - Photodetectors
- Optical I/O module
  - Transceiver Architectures and scalability
- TSV integration with Silicon photonics
- CMOS-SiPh Transceiver Demonstrators
- Conclusion
## OPTICAL vs. COPPER INTERCONNECTS

### TRANSITION ROADMAP (IMEC)

**Optical Interconnects replacing Copper at increasingly Shorter Reach**
- **Datacenter** [5m-10km+]
  - 100G-400G-1.6T+
- **Backplane** [0.5-3m]
  - 8-16-32+ x 50G-100G
- **Board** [5-50cm]
  - 200Gbps+/mm
- **Package** [1cm-10cm]
  - 1Tbps+/mm
- **Interposer/Chip** [1mm-2cm]
  - 10Tbps+/mm

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### Link distance

- **Backplane**
  - Board-to-board [0.5m-3m]
  - Intra-Datacenter [5m-500m+]
  - Inter-Datacenter [10km+]

### I/O Density

<table>
<thead>
<tr>
<th>Distance</th>
<th>Copper</th>
<th>Optical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board</td>
<td>Logic Package-to-Package</td>
<td>Logic-DRAM array [5cm-0.5m]</td>
</tr>
<tr>
<td>Backplane</td>
<td>Logic Core-Core</td>
<td>Logic-DRAM [1mm-5cm]</td>
</tr>
<tr>
<td>Link bandwidth</td>
<td>10Tbps/mm</td>
<td>100Gbps/mm</td>
</tr>
<tr>
<td>Link distance</td>
<td>10Gbps/mm</td>
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<tr>
<td>I/O Density</td>
<td>100Tbps/mm</td>
<td>10Tbps/mm</td>
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### I/O Density

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<thead>
<tr>
<th>Distance</th>
<th>Copper</th>
<th>Optical</th>
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<tbody>
<tr>
<td>Package/Chip</td>
<td>Logic Core-Core, Logic-DRAM</td>
<td>Logic-DRAM [1mm-5cm]</td>
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<tr>
<td>Link bandwidth</td>
<td>1Tbps/mm</td>
<td>1Tbps/mm</td>
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<tr>
<td>Link distance</td>
<td>1Tbps/mm</td>
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<tr>
<td>I/O Density</td>
<td>1Tbps/mm</td>
<td>1Tbps/mm</td>
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</table>

### Source:
- LightCounting
- Intel

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**Source:** LightCounting

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**Source:** LightCounting

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**Source:** LightCounting
OPTICAL I/O MODULE ROADMAP

NEED FOR WAVELENGTH DIVISION MULTIPLEXING

1. Unclear if future CMOS nodes will support baud rates beyond 50Gbd
2. PAM-4 acceptable for long links, but NRZ modulation preferred for short, latency sensitive links
   → At 50Gb/s channel speed, Wavelength Division Multiplexing is essential for module scaling
      • 8+ WDM-channels likely required, even if 2x 8-parallel fibers are used per module → DWDM
SILICON PHOTONIC INTEGRATION

BENEFITS AND DRAWBACKS

Silicon PICs

✓ Fabrication in CMOS fabs [200mm/300mm]
✓ Large Si/SiO$_2$ refractive index contrast of $\sim$2 [scalable PIC density]
✓ Advanced Si patterning capability [193(i), nanometer scale accuracy]
✓ (Si)Ge epitaxy [photodetectors/modulators]
✓ Low resistance contacts to Si [high-speed optical devices]
✓ Volume scalability [>1M units/year] & Efficiencies of scale [cost]
✓ Wafer-scale 3-D packaging and assembly [TSVs, micro-bumps, ...]
✗ No monolithic integrated optical gain/lasing [need for hybrid solution]

Silicon Photonics = Leverage existing CMOS infrastructure for Photonic Integration
IMEC’S SILICON PHOTONICS PLATFORM
50G SILICON PHOTONIC INTEGRATED CIRCUIT TECHNOLOGY

- Co-integration of high performance 50G active and passive blocks in a single platform
- Implemented in 200mm SOI (90/130nm) and 300mm (<28nm)
50G NRZ SILICON PHOTONICS PLATFORM
PASSIVE DEVICES
High index-contrast Si waveguide technology enables compact photonic circuits (\~\mu m bends)
But, more sensitive to sidewall roughness (propagation loss \~ 0.1-1 dB/cm)
FIBER COUPLING INTERFACES
SURFACE NORMAL GRATING COUPLERS

Fiber Grating Couplers: <3dB insertion loss over 30nm optical bandwidth to Standard Single Mode Fiber
FIBER COUPLING INTERFACES

EDGE COUPLERS

- Broadband
- Relatively insensitive for polarization
- Smaller spot size complicate packaging
- Additional process steps and stack layers
- Wafer-scale testing not straightforward

Si Oxy-Nitride Edge Couplers: <2dB insertion loss over 100nm to Specialty Fiber (3um Mode Field Diameter)
SILICON WAVELENGTH MULTIPLEXING DEVICES
RING-BASED DWDM FILTERS

Filter resonance condition
\[ m \cdot \lambda_{res} = L_{RT} \cdot n_{eff} \]
SILICON WAVELENGTH MULTIPLEXING DEVICES

RING-BASED DWDM FILTERS

8+1-channel DWDM Demultiplexing Filter

- Polarization diversity scheme
- 8 channel (de)MUX filter, using cascaded ring filters
- Double-ring filter design with flat-top response
- ~3dB insertion loss, ~20dB crosstalk
- Collective, low-power thermal tuning
50G NRZ SILICON PHOTONICS PLATFORM
SILICON MODULATORS
SIPH OPTICAL MODULATOR OPTIONS

**Si Mach-Zehnder Modulator**

- Optically broadband
- Thermally robust
- Large device (L~1mm)
- Large dynamic power

**Si Ring Modulator**

- Optically narrowband (<1nm)
- Thermally sensitive (<1K)
- Compact device (R~5μm)
- Low dynamic power (1Vpp)

**Ge Si Electro-Absorption Modulator**

- Optical Bandwidth (<30nm)
- Thermally insensitive (<30K)
- Compact device (L~60μm)
- Low dynamic power (2Vpp)
SILICON MACH-ZEHNDER MODULATOR
TRAVELING-WAVE MZM DESIGN AND PERFORMANCE

Parameter | Typ. Value
--- | ---
Operation Wavelength | 1550nm
EO Bandwidth (S21) | f3dB 27GHz (at -1V)
Optical Loss | 8.2 dB/cm (at 0V)
Modulation efficiency | V π 11 V
Optical Insertion Loss | IL -2dB (excludes bias-included loss)
Dynamic Extinction Ratio | ER ~2.2dB (for 2.5Vpp single-ended drive)
Phase-Shifter Length | L 1.5mm

Electro-optic S21 response

50Gb/s Eye diagram with 2.5Vpp
**SILICON RING MODULATOR**

**DESIGN SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Targeted Specifications</th>
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<tbody>
<tr>
<td>Ring radius</td>
<td>5</td>
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<tr>
<td>Quality Factor</td>
<td>2k-10k</td>
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<tr>
<td>Modulation Efficiency</td>
<td>&gt;50</td>
</tr>
<tr>
<td>Modulation Bandwidth $f_{3dB}$</td>
<td>&gt;40</td>
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<tr>
<td>Transmitter Penalty (@1V_{pp})</td>
<td>&lt;6</td>
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<tr>
<td>Heater efficiency</td>
<td>&gt;0.2</td>
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**SILICON RING MODULATOR**

**TYPICAL PERFORMANCE**

<table>
<thead>
<tr>
<th>Q-factor</th>
<th>Voltage swing (-1V to 0.5V)</th>
<th>Modulation efficiency (pm/V)</th>
<th>ER at min TP (dB)</th>
<th>IL at min TP (dB)</th>
<th>Min Transmitter Penalty (dB)</th>
<th>*3dB BW (GHz)</th>
<th>Heating efficiency (nm/mW)</th>
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<tr>
<td>3200</td>
<td>1.5</td>
<td>45</td>
<td>2.6</td>
<td>6.0</td>
<td>11</td>
<td>47</td>
<td>0.284</td>
</tr>
</tbody>
</table>

*Modulation bandwidth reported at wavelength with maximum S21 magnitude

**50G Ring Modulator with Integrated Heater**
SILICON RING MODULATOR ELECTRICAL MODEL
MEASURED S11 VS. ELECTRICAL MODEL FITTING

Electrical equivalent circuit model

- **C_m**: capacitance of metal pads
- **C_Ox, R_Si**: substrate capacitance and resistance
- **C_j, R_s**: capacitance and resistance of RM

**Fitted parameters**

<table>
<thead>
<tr>
<th></th>
<th>Bias</th>
<th>C_j (fF)</th>
<th>R_S (Ohm)</th>
<th>C_Ox (fF)</th>
<th>R_Si (Ohm)</th>
<th>C_m (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fitted value</td>
<td>0V</td>
<td>24</td>
<td>68</td>
<td>49</td>
<td>1100</td>
<td>6.5</td>
</tr>
</tbody>
</table>
### SILICON RING MODULATOR BANDWIDTH VS. TRANSMITTER PENALTY DETERMINED BY RESONANCE QUALITY FACTOR

<table>
<thead>
<tr>
<th>Ring modulator type</th>
<th>Q-factor</th>
<th>Modulation efficiency (pm)</th>
<th>Transmitter Penalty for 1.5Vpp swing (dB)</th>
<th>Measured $f_{3dB}$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-Q</td>
<td>9900</td>
<td>45.2</td>
<td>6.9</td>
<td>16.2</td>
</tr>
<tr>
<td>Medium-Q</td>
<td>3500</td>
<td>61.8</td>
<td>10.1</td>
<td>35</td>
</tr>
<tr>
<td>Low-Q</td>
<td>2200</td>
<td>67.6</td>
<td>11</td>
<td>47</td>
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</tbody>
</table>

**Modulation Bandwidth $f_{3dB}$**

\[
\frac{1}{f_{3dB}^2} = \frac{1}{f_{3dB_{RC}}^2} + \frac{1}{f_{3dB_{Q}}^2} \quad \Rightarrow \quad f_{3dB_{Q}} = \frac{1}{2\pi \tau_r}
\]

\[
f_{3dB_{RC}} = \frac{1}{2\pi RC}
\]

**Trade-off** between Transmitter Penalty and Modulation Bandwidth.
SILICON RING MODULATOR 50-56GB/S NRZ EYE DIAGRAMS

- 50/56G MUX, PRBS 2e31-1, laser power=10dBm
- Measured with 50Ohm terminated probe
- Oscilloscope optical module with 40GHz bandwidth

50Gb/s, 2.5Vpp
Vbias= 0V, ER=5.4dB, SNR=6.8

50Gb/s, 1Vpp
Vbias= 0V, ER=4.7dB, SNR=5.2

56Gb/s, 1.5Vpp
Vbias= -0.25V, ER=4.1dB, SNR=5.2, 1544.67

56Gb/s, 1Vpp
Vbias= 0V, ER=4.5dB, SNR=4.7, 1544.67

50-56Gb/s open eye diagrams from 1Vpp drive swing
GESI ELECTRO-ABSORPTION MODULATOR
WORKING PRINCIPLE & DESIGN

Device cross section, perpendicular to light propagation

Optical absorption vs. wavelength and bias voltage

- **Franz-Keldish effect**: modulate optical absorption coefficient in Ge(Si) by applied electric field
- **Ultra-fast effect (~ps)**, RC limited
- Implemented by reverse-biased p-i-n diode in GeSi waveguide
GESI EAM STATIC MEASUREMENTS
TYPICAL EXTINCTION RATIO, INSERTION LOSS, TRANSMITTER PENALTY

Absorption vs wavelength
GeSi – device (Si = 0.74%)

Static modulator response spectrum
(ER and IL) vs drive swing

Link Power Penalty (LPP) spectrum
vs drive swing

Absorption coefficient increases with applied field
Sub-picosecond effect

ER = 5.3dB and IL =5.2dB
(2Vpp swing at 1555nm)

Optimum operation point close to 1550nm for GeSi EAM (where ER=4.6dB, IL=4.2dB for 2Vpp)

\[
LPP = \frac{P_{\text{out}(1)} - P_{\text{out}(0)}}{2P_{\text{in}}}
\]
GESI EAM STATIC MEASUREMENTS

TEMPERATURE DEPENDENCE

- Operation wavelength shifts with temperature to longer wavelength (0.82nm/K)
- GeSi EAM device is not temperature insensitive beyond ~30K variations
GESI EAM DYNAMIC MEASUREMENTS
SMALL SIGNAL RF PERFORMANCE

- 3dB bandwidth is beyond 50GHz under reverse bias above -1V
- The extracted R, C from EAMs indicate the device speed is RC limited
- The GeSi EAM represents a very small capacitive load of $C_j < 15fF$
- Electrical/Optical response strongly depends on bias voltage and optical power

Electrical $S_{11}$ response

DeviceP (dBm), L(um), V (V), I (mA)
- 0.5, 50.0, -3.0, -1.0
- 0.5, 50.0, -2.0, -0.9
- 0.5, 50.0, -1.4, -0.8
- 0.5, 50.0, -1.0, -0.7
- 0.5, 50.0, -0.8, -0.7
- 0.5, 50.0, -0.4, -0.6
- 0.5, 50.0, -0.2, -0.6
- 0.5, 50.0, 0.0, -0.5

LaserP = 6dBm, L = 50um, W = 500nm
GESI EAM EYE DIAGRAM MEASUREMENTS

56Gb/s NRZ @1550 nm

- Open eye diagram at 56Gb/s NRZ-OOK data rate
- PRBS data stream, length $2^{31}-1$
- Measured with 50Ohm terminated, 50GHz RF probe
50G NRZ SILICON PHOTONICS PLATFORM

GE PHOTODIODE
GE WAVEGUIDE PHOTODETECTOR

GE P-I-N DIODE

- Responsivity: > 0.85A/W at -1V
- O/E 3dB BW > 50GHz
- Dark current: 10nA at -2V
- Capacitance < 20fF

56Gb/s, -2V, 1565nm

Electro-optical S21 response

“VPIN” GePD
IMEC’S SILICON PHOTONICS PROTOTYPING OFFERING
BUILD YOUR OWN PROTOTYPE IN IMEC’S OPEN PLATFORM TECHNOLOGY!

- Accessing imec’s 200mm Si Photonics Platform (iSiPP50G)
  - Both MPW and Fully Dedicated Runs
  - Silicon Validated PDK v2.2.0 is available
  - Supported by various EDA tools
OPTICAL I/O MODULE ARCHITECTURE AND SCALING OPTIONS
PROPOSED OPTICAL I/O MODULE ARCHITECTURE
HYBRID ASSEMBLY ON SILICON PHOTONICS INTERPOSER

Cross Section Schematic

- **DFB LD Array**
- **LC** = Laser Coupler
- **DRV** = Modulator Driver
- **TIA** = Trans-Impedance Amplifier
- **CTRL** = Control Circuit
- **MOD** = Electro-optic Modulator
- **PD** = Photodetector
- **TSV** = Through-Silicon Via
- **MUX** = Wavelength Multiplexer
- **FC** = Fiber Coupler

In-Package Optical Module Integration (400Gb/s+)

- **Switch ASIC/FPGA**
- **Optical Module**
OPTICAL TRANSCEIVER SCALING

Faster Channels

Focus for very-short reach interconnects:
Faster and More Channels

More bits per Symbol
- Amplitude: PAM-X
- Phase and Amplitude: DP-QPSK, QAM-X, ...

More Channels
- Parallel (Single-Mode) Fiber [PSM]
- Multi-Core Fiber, Spatial Division Multiplexing [SDM]
- Wavelength Division Multiplexing [WDM]
OPTICAL CHANNEL SCALING

4-CHANNEL TRANSCIEVER EXAMPLES

**PSM-4**
Parallel Single Mode Fiber

<table>
<thead>
<tr>
<th>Channel</th>
<th>Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>100GbE</td>
<td>4x25Gb/s</td>
</tr>
<tr>
<td>200GbE</td>
<td>4x50Gb/s</td>
</tr>
</tbody>
</table>

**CWDM-4**
Coarse Wavelength Division Multiplexing
OPTICAL CHANNEL SCALING

8-CHANNEL TRANSCIEVER OBJECTIVE

SDM-8
Spatial Division Multiplexing

- Single-λ DFB/FP Laser
- Ge(Si) EAM array
- Multicore Fiber
- Ge(Si) PD array

DWDM-8
Dense Wavelength Division Multiplexing

- Comb DWDM Laser or DFB DWDM Laser array
- Cascaded Ring Modulators
- Cascaded Ring Filters & Ge PDs

<table>
<thead>
<tr>
<th>Channel</th>
<th>Modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>400GbE</td>
<td>8x50Gb/s NRZ or PAM-4</td>
</tr>
<tr>
<td></td>
<td>4x100Gb/s PAM-4</td>
</tr>
<tr>
<td>800GbE</td>
<td>16x50Gb/s NRZ</td>
</tr>
<tr>
<td></td>
<td>8x100Gb/s PAM-4</td>
</tr>
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</table>
TSV INTEGRATION WITH SILICON PHOTONICS
TSV INTEGRATION WITH SILICON PHOTONICS

- 10x100 TSV integration
- Pitch 20-60µm

BSRDL and passivation
TSV
HIGH SPEED PERFORMANCE

Very low RF losses for TSV at 50GHz

High-signal integrity at 50Gb/s NRZ
SIPH TRANSCEIVER DEMONSTRATORS
ULTRA-COMPACT 16X 56GB/S GESI EAM-PD ARRAY

1x16 MMI splitter tree

1 input, 16 TX output
16 RX input

0.7mm

37-channel grid of fiber grating couplers, 37um pitch

61-channel Pitch-Reducing Optical Fiber Array (PROFA, Chiral Photonics)

Input

50um

100x50um GeSi EAM and PD

Diode: 600nm wide, 40um long
PACKAGING

PITCH-REDUCING OPTICAL FIBER ARRAY (PROFA)

PROFA and Packaging by Chiral Photonics
GESI EAM TO GESI PD LOOPBACK TRANSMISSION TEST

16 CHANNEL LINK UNIFORMITY ANALYSIS AT 56Gb/s NRZ

- GeSi EAM array ➔ Dynamic extinction ratio (ER) in the range of 2.7-3.3dB
- GeSi EAM to GeSi PD array ➔ SNR in the range of 3.05-3.92

GeSi EAM optical transmission

GeSi EAM driving voltage (peak to peak): 2.5V, 56Gb/s (PRBS31)
Bias GeSi PD: -2.5V
GESI EAM-PD AT 100GB/S

First SINGLE-WAVELENGTH 100Gb/s NRZ-OOK modulation demo in Silicon Photonics

100Gb/s Eye Diagram for GeSi EAM-to-GeSi PD

Collaboration with
RING MODULATOR DRIVER IN 28NM CMOS
CIRCUIT CONCEPT AND WIRE-BONDED PROTOTYPE

Invertor-based Differential Driver Concept

- Target load per stage: C=150fF
- Target data rate = 50Gb/s (1.1V)
- Voltage swing (~1.7 VDD)
- Single driver supply

Driver supply: VDD=1.1V
E_{bit} = 610 fJ/bit
50Gb/s NRZ
CONCLUSIONS

- Interconnect requirements for high bandwidth density, low-power and low-cost are pushing optical interconnects to shorter distances
- Supporting many modulation schemes & wavelength bands considered for future datacenters single-mode interconnects
- Silicon Photonics for short-reach optical interconnects
  - 50G NRZ optical modulation and detection rates are readily achieved
  - SiPh active devices can be directly driven by advanced CMOS: low capacitance and low drive voltages
  - Tight integration with host CMOS ICs using 3-D assembly
  - Low die cost and volume scalability (Spatial and Wavelength Division Multiplexing)
- Main challenges
  - Low-cost laser array integration on SiPh interposer
  - Self-aligned fiber array assembly
  - Thermal stability (passive and active devices) and optical insertion loss
ACKNOWLEDGEMENT

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Further information available in these papers:

embracing a better life