CDNLIVE℠
Cadence User Conference 2019

View the latest agenda in the mobile app

cadence®

Conference Agenda - Wednesday September 18, 2019

	Custom IC and Analog Grand Ballroom C	Full-Flow Digital Design and Signoff Royal Ballroom H	SoC and System Verification Grand Ballroom B	IP and Block Verification Grand Ballroom A	PCB Design and System Analysis Royal Ballroom I	Cloud-Based Design Royal Ballroom J	IP Solutions Meeting Room 4	Education Services Meeting Room 5
8:45-09:45	Welcome Coffee and Registration - Networking and Designer Expo							
09:45-11:00	**Keynotes** **Anirudh Devgan:** President, Cadence **Shlomit Weiss,** Senior Vice President Silicon Engineering, Mellanox **Anat Shakedd**, Co-Founder and CEO, Nexite **Dov Moran,** Managing Partner, Grove Ventures							
11:00-11:45	Networking and Designer Expo							
11:45-12:15	CUS01 **Technology Overview** *Cadence*	DSG01 **Technology Overview (FED)** *Cadence*	SVG01/02 + IBV01/02 **Technology Overview** *Cadence*		PCB01 **A Platform for System Design and Analysis for 5G and Radar Applications** *Cadence*		IP01 **Choosing a DSP for Hearables** *Cadence*	
12:15-12:45	CUS02 **Technology Overview** *Cadence*	DSG02 **Technology Overview (ICD)** *Cadence*			PCB02 + PCB03 **Introducing New OrCAD 17.4 Release** *EDAis*	Cloud01 + Cloud02 **Rapid Innovation Using Cloud for Design and Verification** *Amazon Web Services with Annapurna*	IP02 **Highly Efficient, Scalable Vision and AI Processors IP for the Edge** *Cadence*	ES01 + ES02 **The New Design Approach: High-Level Synthesis Introduction for RTL Designers** *Cadence*
12:45-13:15	CUS03 **Automated RF and Analog Design** *Intel*	DSG03 **Innovus Mixed Macro Placer** *Mellanox*	SVG03 **Enabling Early FW Development and Debug Using Emulation Platform** *Intel*	IBV03 **Hybrid Verification Approach of Embedded Processor** *Intel*			IP03 **Fusion F1 DSP, Ideal DSP for NB-IoT Modems** *Cadence*	
13:15-14:00	Lunch / Designer Expo / Networking							
14:00-14:30	CUS04 **How We Convert Tool Transition to Success Story!** *Intel*	DSG04 **High-Level Synthesis Will Supercharge Your IP Development** *Intel*	SVG04 **Hybrid Virtual + Emulation SoC Platform for SW-Drivers Validation** *Intel-Mobileye*	IBV04 **Formal Verification of a Custom uController – A Case Study** *Veriest*	PCB04 **Addressing the Challenges of Electrical/Thermal Co-Simulation** *Cadence*	Cloud03 **Lessons Learned from Assisting the Early Adopters of Cloud-Based IC Design** *Cadence*	IP04 **Spring Hill – Intel's Data Center Inference Chip** *Intel*	
14:30-15:00	CUS05 **Mixed Signal Simulation of a 12 bit 50 MS/s Dual Channel Time Domain Two Step ADC** *Analog Value*	DSG05 **BIU Experience: Pegasus and Common UI** *Bar-Ilan University*	SVG05 **Pre-Silicon Verification of an Ethernet Packet Processor with Industrial Strength Traffic Generation** *Marvell*	IBV05 **Enhanced Test Composition and Generation by Integration** *Texas Instruments*	PCB05 **What's New in Electrical Extraction and Analysis** *Cadence*	Cloud04 + Cloud05 **Azure Deployment for Silicon Design** *Microsoft with TSMC*	IP05 **Hearing Sense in Smart Devices** *Alango Technologies*	ES03 **Writing Good SKILL Code** *Cadence*
15:00-15:30	CUS06 **PVS Voltage Aware DRC Using PVL Tcl DFM Property Advance Commands** *TowerJazz*	DSG06 **Equivalence Check with Low Power** *Intel*	SVG06 **Protium Platform Usage in Early SW Bring-Up of SoC** *Altair*	IBV06 **Automotive V Model Verification Flow** *Autotalks*	PCB06 **Multitasking PCB Layout with Several Designers to Reduce Project Time** *Nistec*		IP06 **The Power of Data-Over-Sound** *Sonarax*	
15:30-16:00	CUS07 **Managing Design Traceability for AMS Tapeouts** *ClioSoft*	DSG07 **Implementation of Large Scale Design Changes with Conformal ECO** *Magicleap*	SVG07 **Using PSS to Accelerate Validation Stimuli Development and Execution Efficiency** *Intel*	IBV07 **Modeling DMA in Fake Processors Simulations Using DPI-C** *Satixfy*	PCB07 **Capture Constraint Manager – Front to Back Constraints** *EDAis*		IP07 **Addressing the State of Safety and Security in Today's Vehicles** *Green Hills Software*	
16:00-16:30	Happy Hour in Designer Expo							
16:30-17:30	Best Presentation Awards and Entertainment							