CDN LIVE SM

Cadence User Conference 2019

Shanghai, China—August 15

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AGENDA

08:30 09:30	Registration and Designer Expo							
09:30 09:45	Opening Remark, Sherry Xu, Vice President, General Manager of China and Southeast Asia, Cadence							
09:45 10:15	K01 - Anirudh Devgan, President, Cadence							
10:15 10:45	K02 - Shao-Jun Wei, Professor, Tsinghua University							
10:45 11:15	K03 - Leo Zhu, CEO, YITU Tech							
11:15 11:40	Best Presentation Award Ceremony							
11:40 13:00	Lunch and Designer Expo							
	TRACK 1 **Digital Implementation** 3F, Shanghai Ballroom 2	TRACK 2 **Digital Front-End and Signoff** 3F, Function Room 4	TRACK 3 **PCB Design, IC Packaging, and System Analysis** 3F, Shanghai Ballroom 3	TRACK 4 **System Design and Verification** 3F, Function Room 1	TRACK 5 **Custom IC Design** 3F, Shanghai Ballroom 1	TRACK 6 **Tensilica DSP Ecosystem Partners** 3F, Function Room 3	TRACK 7 **Automotive** 3F, Function Room 2	TRACK 8 **Tensilica Audio DSP New Applications** 3F, Function Room 2
13:00 13:30	DI01 - Achieving Your Best PPA with Cadence Digital and Signoff Solution - *Cadence, Chin-Chi Teng*	DF01 - Genus iSpatial Flow for Best Predictability and PPA - *Cadence, Kam Kittrell*	SP01 - True 3D Analysis of Large Geometries with Clarity 3D Solver - *Cadence, Jian Liu*	SV01 - Optimizing Verification Throughput for a Connected World - *Cadence, Michael Young*	CUS01 - Analog/Mixed-Signal Technology Overview - *Cadence, Zhong Fan*	TIP01 - AI安全与影像应用及趋势 - *旷视科技 Megvii, 沈瑄 产品市场总监*	AU01 - 汽车智能化演进为半导体行业带来的新动力 - *SemiDrive, Jason Zhang*	
13:30 14:00			SP02 - Allegro Pulse and What's New in Allegro 17.4 Release - *Cadence, Julian Sun*	SV02 - Enhance LPDDR5 DRAM Controller Verification with Cadence LPDDR VIP - *Mediatek, Mengru Si*	CUS02 - Meeting Quality and Reliability Requirements for Advanced-Node and Mission-Critical Applications - *Cadence, Rui Pan*	TIP02 - 整合AI产业链，促进算法高效落地 - *极视角 Extreme Vision, 刘若水 战略合作总监*	AU02 - Automotive – The Changing Landscape - *Cadence, Simon Chang*	
14:00 14:30	DI02 - TSMC-Cadence Collaboration on Mobile and HPC Design Enablement Using 5nm Technology - *TSMC, Henry Hsieh*	DF02 - Tempus Hierarchical Techniques and Cloud Computing for STA Signoff and ECO - *Cadence, Marc Swinnen*	SP03 - 2.5D Package Interposer Automatic Design Based on Allegro Package Designer - *GLOBALFOUNDRIES, Cheng Zhang*	SV03 - 基于硬件加速器的高性能芯片仿真与验证 - *IMECAS, Lei Wang*	CUS03 - Analog Mixed-Signal UVM-Based Verification in Automotive Chip - *Analog Device, Steven Xu*	TIP03 - 智能感知与边缘计算 - *臻识科技 Vision-Zenith, 白震东 高级副总裁*	AU03 - Power-Efficient AI and Sensor Processers for Perception and Decision Making in Autonomous Vehicles - *Cadence, Thomas Wong*	
14:30 15:00	DI03 - A Comprehensive Power Optimization Practice on 14nm Chips by Using Innovus Power Recovery Engine - *Avera Semiconductor, Wenxing Jia*	DF03 - Timing and Power Convergence on Mega Chip Using TSO - *Avera Semiconductor, Wei Liu*	SP04 - Overcoming SI/PI Simulation Challenges of LP4/LP4X Interfaces on Mobile Applications - *UniSOC, Nikki Xie*	SV04 - Formal Practice in CPU Core Verification Using JasperGold Formal Verification Platform - *天津飞腾信息技术有限公司, Hongbo Xue*	CUS04 - AMS Verification Method for NXP i.MX RT Product - *NXP Semiconductor, Angela Liang*	TIP04 - Deep Learning Optimization for Edge AI Device - *Skymizer, Samual Liu*	AU04 - Complete Electrical-Thermal Co-Simulation for System Designs - *Cadence, CT Kao*	
15:00 15:15	Tea Break and Designer Expo						AU05 - Addressing the State of Safety and Security in Today's Autonomous Vehicles System Designs - *Green Hills Software, Julia Tang A*	
15:15 15:30	DI04 - Interposer Design with Innovus Implementation System - *ZTE/SANECHIPS, Leqi Li*	DF04 - A True Signoff Solution for Concurrent IR Drop and Timing in Voltus and Tempus Technologies - *Cadence, Jerry Zhao*	SP05 - 面对高速高密需求的软硬结合板的设计与仿真 - *EDADOC, Bruce Wu/Yali Cui*	SV05 - Palladium and PCIe Environment - *Cadence, Allen Pan*	CUS05 - Automatic Simulation Method for Functional Equivalence Check - *YMTC, Lu Liao*	TIP05 - 语音交互引领下的新计算平台 - *声智科技 SoundAI, 李智勇 副总裁&合伙人*	Tea Break and Designer Expo	
15:30 15:45								TA01 - AI-改变世界的力量, The Power of AI - 深聪智能 Smartic, 吴耿源 *联合创始人*
15:45 16:00	DI05 - Low Power Clock Tree Buffer and Inverter Reduction in Innovus Implementation System - *NXP, Glen Ge*	DF05 - 设计中电压降分析与优化 - *Verisilicon, Qing Wang*	SP06 - IPI Simulation Efficiency Improvement Case - *Ericsson, Xiaoli Zhang*	SV06 - FSM Deadlock Hunt Case Study with JasperGold Superlint App - *GLOBALFOUNDRIES, Jun Shen*	CUS06 - UMC 28HPC+ Analog/Mixed-Signal Reference Flow—Cadence Schematic to GDS - *Cadence, Kevin Tsai*	TIP06 - XANC-芯云融合的新一代主动降噪技术 - *会听声学 HTAcoustics, 虞安波*		
16:00 16:15								TA02 - 低功耗语音唤醒方案 - *瑞芯微 Rockchip, 简欢 软件总监*
16:15 16:30	DI06 - 基于innovus提升芯片性能的物理实现方法 - *天津飞腾信息技术有限公司, Shaoxian Bian*	DF06 - A Robust Power Distribution Design with Early PSI Analysis in Voltus IP Power Integrity Solution - *Avera Semiconductor, Hongwei Dai*	SP07 - SerDes Simulation Using IBIS AMI Model - *Teradyne, Gary Wu*	SV07 - 浅谈Emulator在多媒体芯片开发中的应用 - *Goke, Jiguo Zeng*	CUS07 - Introducing the Virtuoso RF Solution for RF System Design - *Cadence, Huanyan Liu*	TIP07 - 智能音箱的音频信号后处理及系统优化 - *索那声美 SONA Acoustic, 李文烨*		
16:30 16:45								TA03 - Low Latency Audio Streaming and Multi Connection Solution - 欧思数码 Optek, 谷石林 副总裁
16:45 17:00	DI07 - Feedthrough of Very Large Scale Integrated Circuit Based on Innovus Implementation System - *ZTE SANECHIPS, Yuebin Xu*	DF07 - InDesign Voltage-Drop Aware Optimization for Accelerating the Design Convergence - *NVIDIA, Chuck Chu*	SP08 - 高速并行信号过孔间的串扰研究 - *NXP Semiconductor, Vector Cheng*	SV08 - Simplify PCIe RP Enumeration Verification Using VIP - *Avera Semiconductor, Fangheng Yu*	CUS08 - Using Virtuoso ADE Verifier in Project Management and Project Regression - *Cadence, Bob Lv*	TIP08 - 基于深度学习的新一代信号处理技术及其应用 - *大象声科 Elevoc, 时晓宽 产品总监*		
17:00 17:15								TA04 - Tensilica HiFi DSP for TWS Solutions - *Cadence, Jeffrey Xu*
17:15 17:30	DI08 - 基于Innovus平台的云端训练AI芯片设计 - *Enflame, Wade Lu*	EDF08 - Electromigration Analysis of FinFET Self-Heating - *Cambricon, Xiaojun Zhang*	SP09 - Automatic Extraction, Verification, and Optimization of 2D and 2.5D Packages - *Avera Semiconductor, Tianhong Lan*	SV09 - Real Number Modeling in Flash Memory Fullchip Validation - *YMTC, Lin Zhou*	CUS09 - Fastest Design Closure with Accurate Parasitic Extraction - *Cadence, Hitendra Divecha*	Lucky Draw		
17:30 17:45								Lucky Draw
17:45 18:00	DI09 - AI in P&R, Mixplacer Introduction - *Broadcom, Necle Zhao*	Lucky Draw	Lucky Draw	Lucky Draw	Lucky Draw			
18:00 18:15								
18:15 18:30	Lucky Draw							