CDN LIVE SM
Cadence User Conference 2019

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CONFERENCE AGENDA

Tuesday, April 2

Time	Front-End Design Room 203	Digital Implementation / Advanced Node Room 209	Signoff Room 201	Custom / Advanced Node Room 210	Mixed-Signal Design Room 204	SI/PI and IC Packaging Room 205	IP and Automotive Room 211	SoC / System Verification Room 207	IP / Block Verification Room 206	PCB Design Room 212
8:30 AM 9:30 AM	REGISTRATION AND BREAKFAST									
9:30 AM 10:10 AM	**FED104** Achieving Optimum Patch Size with Cut Point Flow in Conformal ECO ***Cadence***	**DIG207** Achieving 7nm Complex Block Closure with the Size of 15Mn Instance - A Deep Dive Using Innovus Implementation System ***einfochips***	**SIG101** Using Tempus Scope for Faster Tapeouts ***Avera Semi***	**CUS101** Introducing the Virtuoso RF Solution for RF System Design ***Cadence***	**MIX101** Multi-Dimensional High-Order Yield Analysis for Low-Power SRAM ***Xenergic AB***	**PAC101** Enabling Pin Field Crosstalk Scan for High-Speed Designs ***Xpeedic***	**IPA101** Automotive – The Changing Landscape ***Cadence***	**SOC101 / VER101** Optimizing Verification Throughput for Advanced Designs in a Connected World ***Cadence***		**PCB101** Accelerate PCB Design Layout Using AI and Machine Learning ***Intel***
10:10 AM 10:30 AM	MORNING BREAK									
10:30 AM 12:00 PM	KEYNOTES									
12:00 PM 1:30 PM	LUNCH AND DESIGNER EXPO - MISSION CITY BALLROOM									
1:30 PM 2:10 PM	**FED102** Efficient Conformal Smart LEC Flow for Complex and Big Design at Renesas ***Renesas***	**DIG102** Migrating High-Performance Digital Designs to 7nm/5nm ***TSMC / Cadence***	**SIG102** Accelerating Design Enablement with Advanced Characterization Flows ***MaxLinear***	**CUS102** Automated Structured Tree Routing for Device/Cell Level Using Virtuoso Space-Based Router ***Cadence***	**MIX102** Verifying Low Power in Mixed-Signal Designs Using Formal Method ***Cadence***	**PAC102** 3D Full Wave EM Modeling of IC Packages: A New Approach ***Socionext America***	**IPA102** Rianta Solutions Ethernet Mac and MACSEC IP and VIP ***Rianta Solutions***	**SOC102** Pre- and Post-Silicon Debug and Power Optimization in a 7nm World ***UltraSoC***	**VER102** Automated Configuration of Verification Environments Using Specman Macros ***Veriest Solutions***	**PCB102** Improving Design Quality by Leveraging Factory Digitization ***Aegis Software***
2:15 PM 2:55 PM	**FED103** Hierarchical Scan Architecture for Efficient Test Pattern Deployment ***Barefoot Networks***	**DIG103** Power-Driven Optimization on Arm's Next Advanced Processor Using the Latest Cadence 7nm Digital Flow ***Arm***	**SIG103** Signing Off Largest Networking SoC Designs with Latest Voltus Technologies on Advanced FinFET Nodes ***Juniper***	**CUS103** Sensitive Nets Constraints-Driven Layout ***Analog Devices***	**MIX103** Reusing Your Analog IPs Successfully for Tapeout ***ClioSoft***	**PAC103** Modeling and Simulation Challenges for 16Gbps GDDR6 Interfaces ***Cadence***	**IPA103** Design Methods for Robust Aging Assessment and Validation of Automotive IP ***Texas Instruments, Cadence, and TSMC***	**SOC103** Perspec System Verifier + ISequenceSpec = Spec to Validation Portability ***Agnisys, Inc***	**VER103** Nim and DPI-C and SystemVerilog ***Analog Devices Inc***	**PCB103** Accelerating Design Reuse Methodology for OrCAD Capture-Allegro Flow ***Arista Networks***
3:00 PM 3:20 PM	AFTERNOON BREAK									
3:25 PM 4:05 PM	**FED101** Power-Aware Synthesis Using Genus Low-Power Solution ***Qualcomm***	**DIG104** Concurrent Placement of Macros and Std Cells with the Mixed Placer - Have They Finally Done It? ***Broadcom***	**SIG104** Using Pegasus Verification System for 16nm Tapeout: A Customer Experience ***Texas Instruments***	**CUS104** RF Circuitry CDM Protection Design, Simulation, and Verification ***Qorvo/Magwel***	**MIX104** SKILL Language-Based Cell/Chip-Level ESD Simulation Tool for DTCO and Model-to-Hardware Correlation ***GLOBALFOUNDRIES***	**PAC104** SI and PI Analysis of MCM Module with LPDDR Application ***GLOBALFOUNDRIES***	**IPA104** QoR Analysis Using Aging-Enabled Liberty Variation Format (LVF) Design Flow for Automotive and IoT High-Reliability Applications ***GLOBALFOUNDRIES***	**SOC104** Reducing IC Verification Time by Reusing Stimulus ***Cypress Semiconductor***	**VER104** Formal Verification Applied to an Atypical DV Project ***Broadcom***	**PCB104** PCB Design Rules Standardization to Enable Design Reuse and Shorten Design Cycle ***Motorola***
4:10 PM 4:50 PM	**FED105** I/O Timing Characterization Using a Structural DFT Methodology ***Texas Instruments***	**DIG105** Innovus 19.1 – Machine Learning Innovation Drives Implementation ***Cadence***	**SIG105** Design for Manufacturability (DFM) for the Custom/Analog Design Flow ***GLOBALFOUNDRIES***	**CUS105** Approaches for Simulating Electronic-Photonic Systems with Spectre AMS Designer ***Lumerical***	**MIX105** The Path Towards Battery-Free and Forever Battery Life for Internet of Things ***Atmosic***	**PAC105** Platform PI Design Automation and Optimization upon IFPI-OPI with SPIM and UPIT ***Intel***	**IPA105** Automotive IP Functional Safety: A Verification Challenge ***Cadence***	**SOC105** Virtual Ethernet Design Verification with IxVerify and Palladium Platform ***Keysight Technologies***	**VER105** A Novel Approach to Verifying a PCIe Receiver Framer ***Oski Technology, Inc.***	**PCB105** SerDes DiffPair P/N and Lane Swapping in OrCAD Capture to Allegro PCB Layout Flow ***Arista Networks***
5:00 PM 6:30 PM	EVENING RECEPTION AND DESIGNER EXPO - MISSION CITY BALLROOM									

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Wednesday, April 3

Time	Front-End Design Room 203	Digital Implementation / Advanced Node Room 209	Signoff Room 201	Custom / Advanced Node Room 210	Mixed-Signal Design Room 204	SI/PI and IC Packaging Room 205	IP and Automotive Room 211	SoC / SystemVerification Room 207	Cloud-Based Design Room 212	Academic Room 206
8:30 AM 9:30 AM	REGISTRATION AND BREAKFAST									
9:30 AM 10:10 AM	**FED201** Reduce ECO Turnaround Time by 10X with Conformal ECO Hier-FEF Flow ***Quantenna***	**DIG201** Time to Closure for Physical Design in 16nm ***Texas Instruments***	**SIG201** End-to-End 16nm Signoff Flow with Pegasus DRC, Pegasus LVS, and Quantus Extraction ***AEONSemi***	**CUS201** Meeting Quality and Reliability Requirements for Advanced-Node and Mission-Critical Applications ***Cadence***	**MIX201** Spectre AMS Designer Flex Adoption Reduces the SoC Verification Time ***Cadence***	**PAC201** Power Supply Design Made Simple Using WEBENCH Power Designer, OrCAD, and Allegro PCB Designer ***Texas Instruments***	**IPA201** A 600mV ULP Tensilica Fusion F1 DSP with Low-Voltage SRAMs ***Xenergic AB***	**SOC201** Validation of Tensilica DNA 100 IP's AI Hardware Accelerator by Running Popular NNs on Hardware Emulation Platform ***Cadence***	**CLO201** A Secure Cloud Environment for Government and Commercial Use ***Air Force Research Labs (AFRL)***	**ACA201** Speech Recognition with Scalp Brain Signals ***University of Texas***
10:15 AM 10:55 AM	**FED202** Coverage Closure for HLS-Based Design IP ***Qualcomm***	**DIG202** Pushing the Limit: Improvement of Design Routability in the EUV Technology ***Samsung Electronics***	**SIG202** Liberate AMS Mixed-Signal Interface Characterization for SerDes Design ***Huawei***	**CUS202** Using Generic Custom Device Arrays in the Analog Layout Flow for Advanced Nodes ***Intel***	**MIX202** Verify Fault Detection and Response Table in Mixed-Signal Verification ***Texas Instruments***	**PAC202** Link Channel Mode Conversion and its Impact on 112Gbps PAM4 Systems ***Xilinx***	**IPA202** Samsung Enables Your Next Data Center SoC with Differentiated IP ***Samsung***	**SOC202** System-Level Emulation Performance for Storage Controllers ***Toshiba***	**CLO202** Cloud-Based Innovation for Semiconductor Design ***Amazon Web Services***	**ACA202** Transaction-Level Stimulus Optimization in Functional Verification Using Machine Learning Predictors ***Texas A&M***
10:55 AM 11:15 AM	MORNING BREAK									
11:15 AM 11:55 AM	**FED203** HLS-Based Design Space Exploration for Low-Power Designs ***Intel***	**DIG203** Low-Resistance Routing Methodology in Advanced Technology Nodes Using Innovus PG Router ***Qualcomm***	**SIG203** High-Accuracy Capacitance Extraction Using Quantus Field Solver in MP+Convergence Modes ***Texas Instruments***	**CUS203** Efficient Automotive Verification with Legato Reliability ***Texas Instruments***	**MIX203** Tame Your Analog Mixed-Signal Challenges Through Next-Generation Tools from MathWorks and Cadence ***MathWorks***	**PAC203** Modeling and Simulating 112Gbps SerDes ***Cadence***	**IPA203** Implications of ISO 26262 Edition 2 on Automotive SoC Designs ***SGS-TÜV and Cadence***	**SOC203** Leverage System-Level Emulation for Practical Power Verification and Analysis – Lessons Learned ***Cadence***	**CLO203** STA Signoff of 500M+ 7nm ASIC in the Cloud with Tempus Timing Signoff Solution ***Barefoot Networks***	**ACA203** Enabling Machine Learning Through Ultra-Low-Power VLSI Mixed-Signal Array Processing ***University of Notre Dame***
12:00 PM 1:30 PM	LUNCH AND DESIGNER EXPO - MISSION CITY BALLROOM									
1:30 PM 2:10 PM	**FED204** Genus Early Prediction Flow for Improved SoC Design-Cycle TAT ***Qualcomm***	**DIG204** Mixed Placer: an Unconventional Paradigm for Hard Macro-Intensive Designs ***STMicroelectronics***	**SIG204** Predictable Signoff DRC Runtime with Pegasus Verification System at Advanced Nodes (16nm to 5nm) ***Cadence***	**CUS204** Samsung AMS Reference Design Flow for FinFET and FDSOI Processes ***Samsung***	**MIX204** Pole/Zero-Based Modeling of Analog Filters in SystemVerilog for Subsystem and SoC Verification ***MixSignal Design LLC***	**PAC204** Advanced Package Design Sign-Off Reference Flow ***Samsung***	**IPA204** EMIR (Voltus/Voltus-Fi) Enhancements for GLOBALFOUNDRIES Automotive and RF Qualification ***GLOBALFOUNDRIES***	**SOC204** Maximizing Timing Performance with the Protium S1 Platform ***Plunify Pte Ltd***	**CLO204** Microsoft Azure for Silicon Design ***Microsoft***	**ACA0204** OpenRAM: Enabling Academic Memory Research ***UC Santa Cruz***
2:15 PM 2:55 PM	**FED205** Genus Synthesis 19.1 - New Architectural Compiler Technology Delivers the Best PPA for Advanced IP ***Cadence***	**DIG205** Designing a 7nm Multi-Core Arm Neoverse-N1 System on Chip Using Cadence Implementation Flow and IP ***Arm***	**SIG205** Evaluation of Parametric Timing Yield Using STA ***Qualcomm***	**CUS205** New High-Voltage Simulation Capability in Spectre APS ***Texas Instruments***	**MIX205** Improving TAT in Mixed-Signal Design Implementation ***Cadence***	**PAC205** Electro-Thermal Co-Simulation in Today's Electronics Industry ***Future Facilities***	**IPA205** Power-Efficient AI Processers for Perception and Decision-Making in Autonomous Vehicles ***Cadence***	**SOC205** Towards Secure and Safe Software Development Using Green Hills and Cadence Technology ***Green Hills Technology***	**CLO205** The Cadence Cloud Portfolio ***Cadence***	**ACA205** Next-Generation Chip and System Solutions ***University of Los Angeles***
3:00 PM 3:20 PM	AFTERNOON BREAK									
3:25 PM 4:05 PM	**FED206** Correlation of Calculated Power Between Vectorless and Vector-Based Joules Runs (VCD and Emulation) ***Barefoot Networks***	**DIG206** High-Performance Bus ***Broadcom***	**SIG206** Virtuoso and Innovus Pattern-Based Layout Optimization to Increase Layout Quality ***Cadence***	**CUS206** Polymorphic PDK to Support IP Protection ***SkyWorks***	**MIX206** Liberate AMS Mixed-Signal Interface Characterization for SerDes Design ***Huawei***	**PAC206** Fast and Accurate System Model of DDR4 and Addressing the Challenges of Transition to DDR5 ***Mobiveil***		**SOC206** Optimizing Hardware/Software Development for Arm-Based Embedded Designs ***Arm***	**CLO206** Accelerating Design and Development of Ampere's High-Performance Processors with Palladium Cloud ***Ampere***	
4:10 PM 4:50 PM	**FED207** Managing Multiple Big Projects with a Small Team Using a Cadence Digital Flow ***Jariet Technologies***	**DIG101** Mixed-Signal Design Implementation Using Innovus Implementation System ***Cadence***	**SIG207** QoR Analysis Using Aging-Enabled Liberty Variation Format (LVF) Design Flow for Automotive and IoT High-Reliability Applications ***GLOBALFOUNDRIES***	**CUS207** Review and Customization of Virtuoso Parameterized Layout Generation ***MicroChip***	**MIX207** Machine Learning for Layout Group Prediction ***Cadence***	**PAC207** Challenges and Solutions to Designing Silicon Interposer in SIP Layout ***BroadPak***		**SOC207** Creating a Seamless Cloud-Bursting Environment for Verification ***Methodics***	**CLO207** Moving EDA to the Google Cloud Platform ***Google***	**ACA207** Co-Design of Deep Neural Nets and Neural Net Accelerators ***University of California***
5:00 PM 6:30 PM	CLOSING RECEPTION AND BEST PRESENTATION AWARDS - BALLROOM G									