CDNLIVE SM

Cadence User Conference 2018

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Conference Agenda - Tuesday, April 10

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	Front-End Design	Digital Implementation / Advanced Node	Signoff	Custom / Advanced Node	IP / Block Verification	SoC / System Verification	SI/PI and IC Packaging	PCB Design and Simulation
	Room 203	Room 204	Room 209	Room 210	Room 206	Room 207	Room 208	Room 211
8:30am - 9:30am	Registration and Breakfast							
9:30am - 10:10am	**FED101** Think You're Smart? Try Conformal Smart LEC *Broadcom*	**ADV 101** Case Study: Rapid Implementation of a 7nm Digital IP Test Chip *Arm*	**SIG101** Silicon-Correlated Voltus Power Signoff of Embedded FPGA IPs on Advanced FinFET Nodes *Flex Logix*	**CUS101** Automated Generation of PDK Library Documentation *GLOBALFOUNDRIES*	**IPB 101 / VER101** Cadence Verification Suite: Faster, Smarter Verification *Cadence*		**PAC101** Application-Driven Heterogeneous Integration *BroadPak*	**PCB101** PSpice Systems Option Implementation of Memristor-CMOS Analog Co-Processor *Spero Devices*
10:10am - 10:30am	Break							
10:30am - 12:00pm	Keynotes							
12:00pm - 1:30pm	Lunch and Designer Expo							
1:30pm - 2:10pm	**FED102** Design Implementation of Technology IP Using High-Level Synthesis *Qualcomm*	**ADV102** High-Performance Digital Design at 7nm *TSMC and Cadence*	**SIG102** Taping Out Ultra-Low Power EDGE Computing FPGA on Samsung 28nm FDSOI with Cadence Signoff Tools *Lattice*	**CUS102** Getting Up to Speed on the Latest Virtuoso ADE and Spectre Simulation Tools *Cadence*	**IPB102** The Regression Watchdog: Using vManager Data Mining to Create Real-Time and Offline Reports and Tracking Charts *Western Digital*	**VER102** Pre-Silicon SW/FW Testing with Protium S1 Platform: A Case Study *Microsemi*	**PAC102** Simulate System (Chip-Package-PCB) Power Distribution Network (PDN) Using Sigrity OptimizePI Tool *Seagate*	**PCB102** PSpice and MATLAB Co-Simulation Enables Maximizing DDR Power and Ground Impedance and Minimizing Power Supply Noise *GLOBALFOUNDRIES*
2:15pm - 2:55pm	**FED103** Improving Runtime and PPA via Combinational Logic Pre-Optimization in a CPU Instruction Decoder *D.E. Shaw*	**ADV103** Maximizing PPA on Arm's Next-Gen High-Performance CPU Using the Latest Cadence 7nm Tools and Flow *Arm*	**SIG103** Pegasus Physical Verification Signoff at 16nm *Texas Instruments*	**CUS103** New Ways to Use Your Custom Design Tools in 2018 *Cadence*	**IPB103** Top-Level SoC Mixed-Signal Verification with SystemVerilog EEnet Modeling *Texas Instruments*	**VER103** Towards Systems of Systems Verification – Connecting Design and Test *National Instruments/Cadence*	**PAC103** Enabling System Electrical-Thermal Design *Future Facilities*	**PCB103** Leveraging Virtuoso/MATLAB and PSpice/Simulink Integration for AMS Product Development Roundtrip *MathWorks*
3:00pm - 3:20pm	Break							
3:25pm - 4:05pm	**FED104** Enabling Effective Test of Safety-Critical Memory-Interface Logic for Automotive Applications *Texas Instruments*	**ADV104** Implementation of Innovus Common-UI Flow: a First-Time Cadence User Experience *Broadcom*	**SIG104** Voltus Solution – The Effective Power Integrity Solution for Automotive SoCs and MCUs at Advanced Technology Nodes *Renesas*	**CUS104** Virtuoso Layout Suite EAD: Beyond Aware… *Bosch*	**IPB104** Accelerating SoC Verification Closure with Perspec Portable Stimulus, Xcelium, Palladium, and Protium Platforms *Cadence*	**VER104** Bringup and Debug Challenges of a 16 x Arm Core System, Running Embedded Firmware in a UVM TB *Microsemi*	**PAC104** Temperature- and Geometry-Dependent Analysis of High-Speed PCB Traces *Cisco*	**PCB104** SerDes DiffPair P/N and Lane Swapping in OrCAD Capture to Allegro PCB Layout Flow *Arista Networks*
4:10pm - 4:50pm	**FED105** Case Study: Automated Generation of Function ECO Using Conformal ECO Technology *Quantenna*	**ADV105** Innovus 18.1 Release: Innovation Continues *Cadence*	**SIG105** Convergent Innovus/PVS Hierarchical Metal Fill Flow for 16nm *Microsemi*	**CUS105** Co-Simulation of Integrated Electronic and Photonic Circuits *Lumerical*	**IPB207** High-Performance Arm Processors for Cloud and HPC Server Applications *Cavium*	**VER105** Pioneering High-Performance and High-Fidelity Ethernet Switch Verification for the Networking Market *Cadence*	**PAC105** Brand-New Electrical and Thermal Co-Simulation Analysis *Foxconn*	**PCB105** Reduce Layout Errors and Design Iterations with WEBENCH Power Designer and OrCAD/Allegro Environment *Texas Instruments*
5:00pm - 6:30pm	Reception and Designer Expo							

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Conference Agenda - Wednesday, April 11

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	Front-End Design	Digital Implementation / Advanced Node	Signoff	Custom / Advanced Node	IP / Block Verification	SoC / System Verification	SI/PI and IC Packaging	PCB Design	Mixed-Signal Design and Verification	Tensilica Processors and Design IP	Academic
	Room 203	Room 204	Room 209	Room 210	Room 206	Room 207	Room 208	Room 211	Room 212	Room 202	Room 201
8:30am - 9:30am	Registration and Breakfast										
9:30am - 10:10am	**FED201** Diagnosing a Systematic DFM Issue in a 40nm SoC Device *Microsemi*	**ADV201** Overcoming 7nm PG Challenges *Barefoot Networks*	**SIG201** Quantus FS and Advanced Technology PDKs *GLOBALFOUNDRIES*	**CUS201** Accurate Analog IP Characterization Using Liberate Tools *Microchip*	**IPB201** Architectural Formal Verification of Cache Coherent Protocols *Arteris IP*	**VER201** Delivering on the Promises of Portable Stimulus *TVS*	**PAC201** HSSO: Optimize Serial Link Structures and Automatically Implement Them in Layout *Cadence*	**DES201** Jira Integration into Cadence Design Tools *Motorola*	**MIX201** Mixed-Signal Interoperability for 7nm *Cadence*	**DIP201** Architecting the Most Advanced Automotive SoCs: Maximizing Safety and Performance *NetSpeed*	**ACA201** Application of Machine Learning to EDA Problems *Georgia Institute of Technology*
10:15am - 10:55am	**FED202** Improving Turnaround Time and Automating Verification Flow Development with Conformal Smart LEC *Texas Instruments*	**ADV202** Implementing an IoT Testchip and Software IP for the Arm Platform Security Architecture Using the Cadence Digital Flow *Arm*	**SIG202** Samsung Foundry DFM Flow with Cadence and Next-Generation DFM Solution with Machine Learning *Samsung*	**CUS202** A Surrogate Model-Based Method for Performance Optimization of an Auto-Zero Linear Amplifier *Texas Instruments*	**IPB202** A Scalable VIP to Verify Complex SoCs for High-Traffic Conditions *Broadcom Ltd*	**VER202** Integration and Verification of PCI Express Gen4 Root Complex IP into an Arm-Based Server SoC Application *Arm*	**PAC202** PCIe 5.0: Addressing the Simulation, Test, and Measurement Challenges of 32Gtps *Tektronix*	**DES202** Key Design Considerations that Affect the Cost and Manufacturability of PCBs *TTM Technologies*	**MIX202** Automation of Mixed-Signal Block and Chip-Level Routing Using Innovus Implementation System *Allegro Microsystems/Cadence*	**DIP202** Advanced Semiconductor Processes and High-Performance Memory IP for Automotive Applications *TSMC/Cadence*	**ACA203** Towards Energy-Efficient Information Processing for Autonomous Drive *Arizona State University*
10:55am - 11:15am	Break										
11:15am - 11:55am	**FED203** Design and Verification of Low-Power Flexible 802.11ah IP with Stratus HLS *Adapt-IP*	**ADV203** Cadence Reference Flow Using Samsung Foundry 8nm Signoff Design Methodology *Samsung*	**SIG203** A Novel and Efficient Approach to Model the Substrate Using PVS LVS and QRC for RFIC Design *Towerjazz*	**CUS203** Reducing ECOs with Virtuoso EAD *STMicroelectronics*	**IPB203** Arm and Cadence Partner on ISO 26262 Methodology *Arm*	**VER203** Maximizing ROI of Palladium Platform While Efficiently Managing Complexity Associated with Emulation *Samsung*	**PAC203** Silicon Interposer and Redistribution Layer Interconnect Modeling *Cadence*	**DES203** Batch Checks Aren't Early Enough: Real-Time DFM Checks to Get Done Faster, Sooner *Arista Networks*	**MIX203** Best Practices in Mixed-Signal Modeling and Verification *Cadence*	**DIP203** Automotive Electronics Redefined *Cadence*	**ACA202** Physical Layout for 3D IC Placement and Conditional Routing Rule Management *UC San Diego*
12:00pm - 1:30pm	Lunch and Designer Expo										
1:30pm - 2:10pm	**FED204** Low-Power Signoff Using Conformal-LP Technology *Broadcom*	**ADV204** Power Grid and IR Drop Optimization Using Innovus/Voltus/Pegasus Integrated Solution *Cadence*	**SIG204** Tempus-ECO Solution Significantly Improves Chip's Time to Marketing *HiSilicon*	**CUS204** How to Get Faster and Better Simulation with Spectre Simulation *Cadence*	**IPB204** Coherency Verification of the CHI / CCIX System *Xilinx Inc*	**VER204** Palladium Z1 and Protium S1: The Fastest Way to Make Your System-on-Chip Prototyping a Success Story *Microsemi*	**PAC204** Macromodeling Using Machine Learning Techniques for DDR5 Applications *Cadence*	**DES204** Layer Reduction and 30%+ SI Improvement Using New Via Technology *WUS PCB LTd.*	**MIX204** Verifying Analog-Mixed-Signal Designs with Cadence's Metric-Driven Verification Tools *Texas Instruments*	**DIP204** Addressing PCIe Gen1-5 Test and Debug Challenges with Confidence *Tektronix*	**ACA204** Agile Development of Custom Hardware *UC Berkeley*
2:15pm - 2:55pm	**FED205** Synthesis and DFT Integration for a Mixed-Signal SoC *Boston Scientific*	**ADV205** Clock Implementation on a High-Performance Arm System Using FlexH and Clock Mesh in Innovus and Tempus Solutions *Arm*	**SIG205** Enabling Voltus/Voltus-Fi Solutions for EMIR Power Signoff on GLOBALFOUNDRIES 7LP and 14LPP FinFET Technologies *GLOBALFOUNDRIES*	**CUS205** Virtuoso Layout EAD Routing Techniques *Cadence*	**IPB205** Speedup the Debug Turnaround Time and Regression Run Time with SV Dynamic Test Reload *Microsemi*	**VER205** Pushbutton Prototyping in Days vs Months *NVIDIA*	**PAC205** Model Management and Integration for OrCAD Capture, Allegro, and Sigrity Solutions *Arista Networks*	**DES205** Manufacturing More Efficiently by Using IPC-2581, a Contract Manufacturer's Success Story *Axiom*	**MIX205** An EDA Tool for Static Crosstalk Analysis in Mixed-Signal Designs *Texas Instruments*	**DIP205** Achieving ASIL-B Readiness with Tensilica Configurable Processor IP *Cadence*	**ACA205** A Self-Powered IoT SoC Platform for Wearable Health Care *Wayne State University*
3:00pm - 3:20pm	Break										
3:25pm - 4:05pm	**FED206** Integrated Genus, Innovus, and Tempus Flow to Reduce Metal Cost on a 16nm Design *MaxLinear*	**ADV206** Power-, Performance-, and Area-Optimized Implementation of 802.11.ax MAC Core Using Innovus Multi-Tap CTS *Broadcom*	**SIG206** Virtuoso Platform-Based Unified Design Finishing Solution for GF 7LP *GLOBALFOUNDRIES*	**CUS206** Optimizing Via Placements Through Techfile and Automation *Texas Instruments*	**IPB105** Rapid Testbench Setup in an AMS UNL Flow for Mixed-Signal Verification *Texas Instruments*	**VER206** Integration of vManager Platform with Industry Standard "DOORsNG" to Address Requirement Traceability *NXP Semiconductor*	**PAC206** IBIS-AMI for PCI Express Gen 4 *IBM*	**DES206** Electrical Engineers and PLM, How to Make It Work *XLPM*	**MIX206** Mixed-Signal Verification Challenges and Solutions *Broadcom*	**DIP206** Enabling High-Speed Interface IP on Samsung Foundry 10LPP Process for Enterprise Applications *Samsung/Cadence*	**ACA206** Design and Synthesis of Trusted FeFET-Based Microelectronics for DO-254 Assurance *University of Mississippi*
4:10pm - 4:50pm	**FED207** Synthesis Through Implementation Challenges and Solutions for a Large Networking Chip *Broadcom*	**ADV207** Body-Bias Interpolation in 22FDX Using Innovus, Tempus, and Voltus Solutions *GLOBALFOUNDRIES*	**SIG207** Simultaneous Switching Inputs: Covering a Significant Hold Margin Risk in Tempus Solution *Inphi*	**CUS207** 7nm Custom Design Reference Flow Based on Virtuoso WSP (Width Spacing Pattern) *GLOBALFOUNDRIES*	**IPB206** Introducing Next Generation Engineering Compute: Building the EDA Stack on Arm *Qualcomm*	**VER207** Enabling Full Design Lifecycle Hardware/Software Security Verification *Tortuga Logic*	**PAC207** Optimizing FPGA-HBM Non-TSV Interposer Design *Xilinx*	**DES207** How to Design Boards that Work the First Time *FEDEVEL*	**MIX207** Demystify Mixed-Signal Simulation Errors *Texas Instruments*	**DIP207** ASIL-Ready Processor IP and ISO 26262 Part 11 *Cadence*	**ACA207** Neural Network Acceleration on Conventional Platform and Neuromorphic Fabric *Duke University*
5:00pm - 6:30pm	Closing Reception and Best Presentation Awards										