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Cadence User Conference 2019
EMEA – Munich, Germany—May 6-8

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Monday, May 6

	Full-Flow Digital Design and Signoff Room Ammersee II	Custom IC Design and Verification Room Ammersee I	Mixed-Signal and Advanced Methodologies Room Alpsee	SoC Design and Verification Room Chiemsee	Signal and Power Integrity Analysis Room Bodensee I	Automotive and IP Solutions Room Schliersee	Academic Room Pilsensee
12:00	Registration Opens						
12:00 - 13:30	Light Lunch Buffet and Designer Expo						
13:30-14:00	**DSG01** The Challenge of Designing a "First-Time-Right" Wi-Fi HaLow Baseband in Less than Six Months ***Methods2Business***	**CUS01** PVS Voltage Aware DRC Using PVL Tcl DFM PROPERTY Advance Commands ***TowerJazz***	**MS01** Experiences in OpenAccess Interoperability with Virtuoso and Innovus Solutions for Mixed-Signal Designs ***Infineon Technologies***	**SVG01** Full-Chip System-on-Chip Emulation Using Palladium Z1 Emulation Ecosystem ***Dream Chip Technologies GmbH***		**ASIP01** Automotive System Enablement ***Cadence***	**AC01** Updated Cadence 2019 Portfolio Available for European Academics via Europractice ***Science and Technology Facilities Council***
14:00-14:30	**DSG02** I2C PAD Characterization Methodology Using Liberate Characterization ***Dialog Semiconductor***	**CUS02** A New Methodology for Active Substrate Parasitic Extraction in Automotive HV-CMOS Processes ***X-FAB Semiconductor Foundries GmbH***	**MS02** Fast Implementation of Small Digital Blocks Within a Custom Layout Environment ***ams AG***	**SVG02** Hybrid Virtual + Emulation SoC Platform for SW-Drivers Validation ***Intel-Mobileye***	**WKSH1** How to Perform Power Integrity Analysis of a Motor Control Unit by Combining Sigrity and PSpice Technology ***Cadence FlowCAD***	**ASIP02** Addressing the State of Safety and Security in Today's Autonomous Vehicles System Designs ***Green Hills Software***	**AC02** Lead Institution for Analog Design Automation: New Thoughts in EDA for Analog ***Reutlingen University - Robert Bosch Center for Power Electronics***
14:30-15:00	**DSG03** Leveraging IJTAG for a Complex Mixed-Signal Design ***Kandou Bus S.A***	**CUS03** Precise Layout Area Estimation of Analog/Mixed-Signal Circuits ***STMicroelectronics***	**MS03** Automated DfM Optimization Using Pattern Matching in Virtuoso and Innovus Solutions ***NXP Semiconductors***	**SVG03** Fast Processor Models for Software Bring Up and Hardware-Software Co-Verification ***Imperas Software***		**ASIP03** A Configurable Fault-Tolerant Multicore System Based on Tensilica Fusion G3 DSPs ***IHP***	**AC03** IC Layout Automation with Self-Organized Wiring and Arrangement of Responsive Modules (SWARM) ***Reutlingen University***
15:00-15:30	**DSG04** RTL-Based Power Calculation with Joules RTL Power Solution ***VSORA***	**CUS04** Interactive Resistance Measurement for Hierarchical Layout Nets ***NXP Semiconductors***	**MS04** Design Flow and Technology Demonstrator for 60GHz WiGig Antenna Array on Package ***GLOBALFOUNDRIES***	**SVG04** Dynamic Software Analysis in Virtual Platforms ***Ericsson***		**ASIP04** A Tool to Ease Design-Space-Exploration Using the Tensilica LX7 ASIP ***Ruhr-Universität Bochum***	**AC04** SPAM - A SKILL Package Management System ***Reutlingen University***
15:30-16:00	Coffee Break						
16:00-16:30	**DSG05** Conformal Smart LEC Results on ST ADG Devices ***STMicroelectronics***	**CUS05** Design Intent - A Path Towards Better Communication Within IC Design Teams ***Robert Bosch GmbH***	**MS05** EM_ICT Enhancements for RF Qualification ***GLOBALFOUNDRIES***	**SVG05** Modem Baseband SoC Architecture Exploration and Validation in the SAVE Framework ***Intel***		**ASIP05** Power-Efficient AI Processors for Perception and Decision-Making in Autonomous Vehicles ***Cadence***	**AC05** Lead Institution for Embedded Systems Design and Verification: Development of Adaptive Dependable and Robust Systems ***Brandenburg University of Technology (BTU) Cottbus – Senftenberg***
16:30-17:00	**DSG06** Improving Leakage and Dynamic Power of High-Performance Arm Cortex-A76 Core Using Cadence Solutions ***Arm***	**CUS06** Fast Design and Reuse of Analog IP Using Intelligent IP Generators and Virtuoso Technology ***Fraunhofer IIS/EAS***	**MS06** Quality Assurance in the Verification of Power Grid of X-FAB's Memory Compilers with Voltus-Fi Flow ***X-FAB Semiconductor Foundries GmbH***	**SVG06** PSS - Automotive Case Study ***Infineon Technologies***	**WKSH1 Cont'd** How to Perform Power Integrity Analysis of a Motor Control Unit by Combining Sigrity and PSpice Technology ***Cadence FlowCAD***	**ASIP06** AI Inference at the Edge – The Realities of Hardware and Software Integration ***Cadence***	**AC06** PSS: Gearing Up for Large-Signal Simulation ***Ghent University - imec***
17:00-17:30	**DSG07** Accelerating Timing Closure Using In-Design Track-Based Metal Fill with Innovus Implementation System ***STMicroelectronics***	**CUS07** RF Simulation Techniques for Analog Circuits ***Dialog Semiconductor***	**MS07** Visualize and Prevent EM Effects in Automotive Designs Using Voltus-Fi Custom Power Integrity Solution ***Melexis***	**SVG07** Using Perspec System Verifier in the IP Verification of the Aurix2G RADAR Signal Processing Unit ***Infineon Technologies***		**ASIP07** Real-Time LED Flicker Mitigation on a Tensilica Vision DSP for Digital Side Mirror Systems ***Leibniz University Hannover***	**AC07** Application of Cell-Aware Test on an Advanced 3nm CMOS Standard-Cell Library ***imec***
17:30-18:00	**DSG08** M1 vs Poly Pitch: Gear Ratio Change ***imec***	**CUS08** Optimizing Spectre APS Transient Speed and Convergence ***Texas Instruments***	**MS08** Printer Application IC - Analog on Top Flow with LVDS Signal Balancing Through EAD ***STMicroelectronics***	**SVG08** TOP-Level Verification Challenges for Interconnect and Closing the Gap Using IWB/IVD ***Ericsson***		**ASIP08** Mixed-Signal Analysis and Verification to Meet ISO 26262 Safety Requirements ***Texas Instruments***	**AC08** MEMS-IC Yield Optimization with Electrical and Mechanical Process Parameters ***Technical University of Munich***
18:00-20:00	Networking Buffet and Designer Expo						

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Tuesday, May 7

	Full-Flow Digital Design and Signoff Room Ammersee II	Custom IC Design and Verification Room Ammersee I	Mixed-Signal and Advanced Methodologies Room Alpsee	SoC Design and Verification Room Chiemsee	Multi-Fabric Design and Analysis Room Bodensee I	PCB Design and Analysis (German/Deutsch) Room Bodensee II	Automotive and IP Room Schliersee	Academic Room Pilsensee	Special Sessions
07:30-08:45	Welcome Coffee and Registration								
8:45-10:00	Keynotes Tom Beckley: Senior Vice President and General Manager, Custom IC & PCB Group, Cadence Hans Adlkofer, Vice President Automotive System Group, Infineon Technologies								
10:00-10:30	Coffee Break								
10:30-11:00		CUS09 Verification of High-Level Design Requirements with Virtuoso ADE Verifier *ams AG*	MS09 Real-Number Modeling of Loading Effects in Power Regulation Using SV ENet *Texas Instruments*	SVG09 Formal Verification Signoff for Digital IP: A Comparison Between Classical UVM Versus Formal Based *STMicroelectronics*	SPB01 Cross-Fabric Design Planning and Optimization, Taking into Account the Package Routing Strategy *STMicroelectronics*	PCB01 What's New im PCB Flow (Front End) *FlowCAD*	ASIP09 112G SerDes for 400G/800G Networking *TSMC and Cadence*	AC09 Lead Institution for System-Level Design: Heterogeneous Runtime Adaptive Multicore Architectures for Autonomous Systems *Technical University Dresden*	CL01 Cadence Cloud/The Future of Electronic Design Automation *Cadence* Room Eibsee
11:00-11:30	DSG09 New Technology Innovations in the Cadence Digital Flow *Cadence*	CUS10 Implementing a Grid-Based Design Methodology to "Design Out" the Impacts of Shrinking Nodes *IC Mask Design*	MS10 UVM ATE Tester Probe UVC for Top-Level Mixed-Signal Verification *Texas Instruments*	SVG10 A Comprehensive and Reusable Strategy to Verify Cores Based on UVM and Formal Verification *STMicroelectronics*	SPB02 Checking the Connectivity Between Design Fabrics *STMicroelectronics*	PCB02 What's New im PCB Flow (Back End) *FlowCAD*		AC10 Formal Verification with Broad-Spectrum ANSI-C Reference Specifications *University of Oxford*	
11:30-12:00		CUS11 Technology Overview *Cadence*	MS11 Chip-Level Verification of RF-AMS SoCs *Innowicom System Solutions AB*	SVG11 Formal Verification in the Context of Highly Configurable IPs *Texas Instruments*	SPB03 Virtuoso Platform as a Common Layout Design Environment for Chip/Package/PCB Co-Design *Infineon Technologies*	PCB03 System Design *FlowCAD*	ASIP11 CNN Design Space Exploration on Tensilica Vision P6 DSP *Leibniz University Hannover*	AC11 Master Thesis Contest Winner: Automated Design Space Exploration of Digital Audio Processors for Hearing Aids *Leibniz University Hannover*	CL02 Cloud-Based Innovation for Semiconductor Design *Amazon Web Services* Room Eibsee
12:00-12:30	DSG10 Mixed Placer: An Unconventional Paradigm for Hard Macro-Intensive Designs *STMicroelectronics*		MS12 Path-Based Timing Verification Flow for Full-Custom Circuits *IBM*	SVG12 Accelerate DFT Simulations with Xcelium Multi-Core Technology *STMicroelectronics*	SPB04 Applying Team Design and DFM Checking to IC Package and SiP *Cadence*	PCB04 Unternehmensweites PCB-Daten-Management *FlowCAD*	ASIP12 Multiframe Imaging on Tensilica Vision P6 DSP *Visidon*	AC12 Synthesis and Test of IP-Blocks with Fault Mitigation *Saint Petersburg State University of Aerospace Instrumentation (SUAI)*	
12:30-13:30	Lunch and Designer Expo								
13:30-14:00	DSG11 Designing a 7nm Multi-Core Arm Neoverse-N1 System on Chip Using Cadence Implementation Flow and IP *Arm*	CUS12 Legato Reliability Fault Simulation - An Automotive Safety Case Study *Melexis*	MS13 Technology Overview *Cadence*	SVG13 High-Level Synthesis Models in Pre-Silicon Verification *Intel*	SPB05 Implementation of Complex Packaging Design Rules and Layout Optimization Using RAVEL Algorithms in Cadence SiP *STMicroelectronics*	PCB05 Integrierte Neue Design Checks *FlowCAD*	ASIP13 A Low-Power Tensilica Fusion F1 DSP and Low-Voltage SRAMs Achieving 400MHz at 600mV *Xenergic*	AC13 Lead Institution: University of Lübeck *University of Lübeck*	WOM01 12% Is Not Enough, Changing Industry to Support Women in Engineering *Women's Engineering Society* Room Walchensee
14:00-14:30	DSG12 How to Improve TAT and PPA by Using Design Metrics *Socionext Europe GmbH*	CUS13 Reliability Analysis Results Parsing Flow *Xilinx*	MS14 Implementing Checks for Power Domain Crossings on Schematic Level *RacyICs*	SVG14 Accelerating Verification of RF Chips for 5G *Infineon Technologies*	SPB06 25Gbps Simulations with Sigrity 2018 Release *Grass Valley*	PCB06 Integrierte Design Analyse *FlowCAD*	ASIP14 Case Study: Design Methodology for Optimized GPS IP Solution Using Tensilica DSP *Nestwave*	AC14 Reliability, Security and Quality in Nanoelectronic Systems – Update from Cadence Early Stage Researchers *Cadence*	WOM02 Interactive Session: Breaking the Mould *Women's Engineering Society* Room Walchensee
14:30-15:00	DSG13 Challenges in Digital Implementation of a Huge Sensor Array Design with High-Speed SerDes Interface *Fraunhofer IIS*	CUS14 Degradation Model Creation Flow *Fraunhofer IIS*	MS15 DARE SET Simulation Flow Integrated in Virtuoso Analog Design Environment *imec*	SVG15 A Python Client Library for vManager API *EXTOLL GmbH*	SPB07 Electrical/Thermal Co-Simulation of SMPS High Current Density PCB Design *Infineon Technologies*	PCB07 Full Wave 3D Simulations *FlowCAD*	ASIP15 Smart Hearing Aid Processor with Ultra-Low Power Consumption *Dream Chip Technologies GmbH*	AC15 Master Thesis Contest Winner: Procedural Capacitor Placement and Routing in Charge Redistribution ADCs with Generalised Capacitor Ratios by Nonlinearity Analysis Considering Parasitics *Technical University of Munich/Infineon Technologies*	
15:00-15:30	Coffee Break								

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15:00-15:30	Coffee Break							
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15:30-16:00	**DSG14** A Flow for Early Power Analysis Using Joules and Voltus Solutions ***Analog Devices***	**CUS-Demo I** Getting the Most Out of Virtuoso ADE in Virtuoso 18.1 Release ***Cadence***	**MS-Demo I** Best Companions: vManager Platform and Virtuoso ADE Verifier - Leading-Edge Technology and Methodology for Mixed-Signal Verification Closure ***Cadence***	**SVG16** Technology Overview ***Cadence***	**SPB08** SI/PI/EMC Full System Simulation of Complex Tester PCB Boards (40 Layers) MLO, Contact Unit and IC ***NXP Semiconductors***	**PCB08** Starrflex (Rigid Flex) Technologie ***Würth Elektronik GmbH & Co. KG***	**ASIP16** Advanced Memories: Design Decisions for Advanced Memory Interfaces ***Arm and Cadence***	**AC16** Workshop: Rapid UVM-e Testbench Generation ***Cadence***
16:00-16:30	**DSG15** Die/Package Co-Design in 28FDOI Technology Using Voltus-Sigrity Package Analysis ***STMicroelectronics***	**CUS-Demo II** Advanced Methodologies in Virtuoso 18.1 Release: Concurrent Layout Editing, Design Planner, Simulation-Driven Routing ***Cadence***			**SPB09** Introducing a 5G Reference Design ***Cadence***	**PCB09** Starrflex (Rigid Flex) Technologie (Live Demo) ***FlowCAD***	**ASIP17** Implementing LPDDR5 Controller and PHY for Mobile, Automotive, and Computing Applications ***Cadence***	
16:30-17:00	**DSG-Demo I** Smart Digital Implementation Using Innovus Machine Learning ***Cadence***	**CUS-Demo III** Addressing Complex Low-Power Design and Verification Challenges Using Virtuoso Power Manager ***Cadence***	**MS-Demo II** Spectre AMS Designer Flex Use Model Reduces SoC Verification Time ***Cadence***	**SVG17** Emulation Automation Workflow: Your Way to Success ***Arm***	**SPB10** True 3D Analysis on Large Geometries with Clarity 3D Solver ***Cadence***	**PCB10** Embedded Components ***AT&S Deutschland GmbH***	**ASIP18** Enabling High-Performance Computing Applications with Differentiated IP and Bleeding-Edge Semiconductor Processes ***Samsung***	**AC17** New Stars on the Horizon – Innovative Startups Showcase Their Vision ***Xenergic, MAGICS, and aiCTX***
17:00-17:30	**DSG-Demo II** Bus Guides and Timing Closure with Innovus High-Frequency Router ***Cadence***	**CUS-Demo IV** Legato Reliability Solution ***Cadence***	**MS-Demo III** Analog and Mixed-Signal Functional Safety Flow Through vManager Metric-Driven Signoff Platform ***Cadence***		**SPB11** Avoid Unnecessary Iterations with Your Manufacturing Partner – A New Approach to Reducing or Eliminating TQs and Accelerating Your New Product Introduction ***Multek, A DSBJ Company***	**PCB11** Embedded Components (Live Demo) ***FlowCAD***	**ASIP19** IP Portfolios for Automotive and High-Performance Computing Designs ***Cadence***	
17:30-18:30	Designer Expo							
18:30-20:00	Dinner and Best Presentation Awards							
20:00-23:00	Evening Event							

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Wednesday, May 8

	Full-Flow Digital Design and Signoff Room Ammersee II	Custom IC Design and Verification Room Ammersee I	Mixed-Signal and Advanced Methodologies Room Alpsee	MCAD-ECAD Room Bodensee I	SoC Design and Verification Room Chiemsee
08:00-08:30	Welcome Coffee and Designer Expo				
08:30-09:00	**DSG-Techtorial I** IR Drop Analysis and Optimization in Innovus Implementation System ***Cadence***	**CUS-Techtorial I** High Performance Global Remote Access to Cadence EDA Software ***OpenText***	**MS-Techtorial I** Managing AMS Designs for Successful Tapeouts ***ClioSoft***	**WKSH2** Library Part Creation ***FlowCAD***	**SVG-Techtorial** Do More with Less – Optimizing Your Throughput ***Cadence***
09:00-09:30		**CUS-Techtorial II** Virtuoso RF Solution: A Comprehensive RF Flow for IC, Package, and Module Design ***Cadence***	**MS-Techtorial II** Using SystemVerilog EEnet to Model Complex Electrical Networks ***Cadence***		
09:30-10:00					
10:00-10:30	**DSG-Techtorial II** Genus and Modus Solutions: Deep Dive into Hierarchical Test ***Cadence***	**CUS-Techtorial III** Design of a Photonic Lidar Module in a New Unified Electronics-Photonic Design Environment ***Lumerical and Cadence***	**MS-Techtorial III** Advanced MS Verification of Multi-Disciplinary Systems with SV UDN-2-UDN/ Logic/Real ***Cadence***		
10:30-11:00	Coffee Break and Designer Expo				
11:00-11:30	**DSG-Techtorial III** Genus and Innovus Solutions: Physical Flows for Best PPA and Predictability ***Cadence***	**CUS-Techtorial IV** Writing Good SKILL Code ***Cadence***	**MS-Techtorial IV** Using Quantus SmartView to Accelerate Post-Layout Analysis of Parasitics and Electromigration (EM) ***Cadence***	**WKSH2** Library Part Creation ***FlowCAD***	
11:30-12:00			**MS-Techtorial V** Electrostatic Discharge (ESD) Analysis with Voltus-Fi Custom Power Integrity Solution ***Cadence***		
12:00-12:30	**DSG-Techtorial IV** IP...The Challenge of the Deliverables ***Cadence***	**CUS-Techtorial V** Custom Silicon Design Automation with Cadence PCell Designer ***Robert Bosch GmbH***	**MS-Techtorial VI** Accelerated Design, Migration, and Substrate Coupling for Analog Design ***Intento Design***		
12:30-13:00		**CUS-Techtorial VI** Cadence Cloud: A Secure and Flexible Solution to Enable Engineering Productivity and Accelerate Time to Market ***Cadence***	**MS-Techtorial VII** Tame Your Analog Mixed-Signal Challenges Through Next-Generation Tools from MathWorks and Cadence ***MathWorks***		
13:00-14:30	Lunch and Designer Expo				