CDN LIVE℠
Cadence User Conference

Conference Agenda, Monday, May 7

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	Full-Flow Digital Design and Signoff	Custom	Mixed Signal and Advanced Methodologies	SoC Design and Verification	PCB Simulation	Automotive and IP Solutions	Academic Track
	Room Ammersee II	Room Ammersee I	Room Alpsee	Room Chiemsee	Room Bodensee I	Room Schliersee	Room Pilsensee
12:00 13:30	Registration Opens and Light Lunch Buffet						
13:30 14:00	**DSG01** So How Can the HLS Flow Help You Cut TTM? *Cadence*	**CUS01** Lifetime Verification by Circuit Level Aging Simulations *Fraunhofer Institute*	**MS01** Demystify the Mixed-Signal Simulation Errors *Texas Instruments*	**SVG01** Performance Modeling for LPDDR4 Memory Subsystems Using SystemC and Approximately-Timed TLM *Cadence*		**ASIP01** Addressing IP Management and Traceability Challenges for ISO 26262 *Methodics*	**AC01** Updated Cadence 2018 Portfolio Available for European Academics via Europractice *Science and Technology Facilities Council*
14:00 14:30	**DSG02** Latency-Constrained Design for a Display Stream Compression Decoder with Stratus HLS *Socionext*	**CUS02** Case Study of Well Proximity Effects in 180nm *ams AG*	**MS02** A Portable Environment for Mixed Signal Verification *STMicroelectronics*	**SVG02** A Deep Dynamic Formal Verification-Based Approach for Complex Systems-on-Chip *Ruhr-University Bochum*		**ASIP02** Addressing PCIe Gen1-5 Test and Debug Challenges with Confidence *Tektronix*	**AC02** SW/HW System Co-Design Enablement for Coarse-Grain Heterogeneous Manycore Platforms *Saint Petersburg State University of Aerospace Instrumentation*
14:30 15:00	**DSG03** Inter-Module Matrix: A Metric-Driven Approach to Improving RTL Quality *Arm*	**CUS03** Quantus FS and Advanced Technology PDKs *GLOBALFOUNDRIES*	**MS03** An Efficient SKILL Based DB for Design Electrical Analysis *STMicroelectronics*	**SVG03** Interactive Visualization of Virtual Platform Coverage *Cadence*		**ASIP03** The System Approach to Voice Enhancement for Automatic Speech Recognition in IoT Devices. *Alango Technologies*	**AC03** Processor Architecture Tradeoffs for On-Site Electronics in Harsh Environment *Leibniz Universität Hannover*
15:00 15:30	**DSG04** RTL Stimuli Based Power Calculation with Joules RTL Power Solution *Renesas Electronics*	**CUS04** Recent Enhancements in Quantus Extraction Solution and its Integrated Capacitance Field Solver Allow New Applications *Infineon Technologies*	**MS04** XPS/Flash - A New Option for High Performance Flash Design Verification *X-FAB Semiconductor Foundries*	**SVG04** Augmented Reality and Rapid-Prototyping Based Supervision and Maintenance of an Industrial Process *Ruhr-University Bochum*	**ICSIG01** Application of OrCAD Capture with PSpice as a Tool for Analog Circuit Diagnosis *Technical University of Sofia*	**ASIP04** Designing DRAM Interfaces for Automotive Electronics *Cadence*	**AC04** Evaluation of Heterogeneous Tool Chains for Building Complex FPGA-Based MPSoCs *IHP Microelectronics*
15:30 16:00	Coffee Break						
16:00 16:30	**DSG05** Full Chip Power Signoff using the Voltus OnChip Voltage Regulator Flow *ams AG*	**CUS05** Constraint-Aware Simulation with Virtuoso ADE Checks/Asserts *Infineon Technologies*	**MS05** A Flexible and Full Cadence Flow for Mixed Simulation *STMicroelectronics*	**SVG05** SRISA Protium S1 Approach *SRISA*	**ICSIG02** Checking Compliance on the Complete System by Integrating Signal, Power, and Thermal Integrity Analysis for PCB and IC Package *Cadence*	**ASIP05** Enabling High Speed Interface IPs on Samsung Foundry 10LPP Process for Enterprise Applications *Samsung*	**AC05** Visual Programming Environment for Cadence SKILL *Reutlingen University*
16:30 17:00	**DSG06** Automation of Mixed-Signal Block and Chip-Level Routing Using Innovus Implementation System *Allegro MicroSystems*	**CUS06** EM Check on Poly Resistor Device and RF FET Using Voltus-Fi Custom Power Integrity Solution *GLOBALFOUNDRIES*	**MS06** A Digital-Centric Real Number Modelling Based Mixed-Signal Design Flow *EXTOLL*	**SVG06** Amber – A TLM IP Library for Rapid System Prototyping *Cadence*		**ASIP06** An Area and Leakage Efficient Multi-Port SRAM for Near-Threshold GHz Operation *Xenergic*	**AC06** Design Flow Automation for On-Chip Inductors *University of Heidelberg*
17:00 17:30	**DSG07** Conformal-ECO: How to Recover Six Weeks to PG *Texas Instruments*	**CUS07** Virtuoso Layout Suite EAD, Beyond Aware… *Robert Bosch*	**MS07** Aspects of Library Characterization of Digital Standard Cells with Complex Circuit Topology *IHP Microelectronics*	**SVG07** Improving Design Flow by Automating TLM Model Generation and Applying Existing RTL Based Verification *Renesas Electronics*	**ICSIG03** Planning and Considering Power Supply Design for a DDRx Analysis *Cadence*	**ASIP07** A 0.5V - 0.8V Tensilica HiFi Mini in 40nm LP *Minima Processor*	**AC07** Impedance Matching Network Synthesis Toolbox for Cadence *Vilnius Gediminas Technical University*
17:30 18:00	**DSG08** Hierarchical Timing Closure with Tempus Scope Models *Cadence*	**CUS08** Reducing ECO's with Virtuoso EAD *STMicroelectronics*	**MS08** System-Level Operating Condition Checks: Automated Augmentation of VerilogAMS Models *IMMS*	**SVG08** UVM-ML Testbench for TLM2.0 Models *Cadence*		**ASIP08** Virtual Prototyping of Convolutional Neural Networks with Tensilica IP *Ruhr-University Bochum*	**AC08** Teaching Microelectronic Design by Doing *Università degli Studi di Cagliari*
18:00 20:00	Networking Buffet and Designer Expo						

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Conference Agenda, Tuesday, May 8

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07:30 08:45	Welcome Coffee and Registration							
08:45 10:00	**Keynotes** **Paul Cunningham, Corporate VP and GM, System and Verification Group (SVG)** **Prof. Dr.-Ing. Philipp Slusallek, Scientific Director at the German Research Center for Artificial Intelligence (DFKI)** **"Understanding the World with AI: Training and Validating Autonomous Vehicles Using Synthetic Data"**							
10:00 10:30	Coffee Break							
	Full-Flow Digital Design and Signoff	**Custom**	**Mixed Signal and Advanced Methodologies**	**SoC Design and Verification**	**Package and Board Design and Analysis**	**PCB Design and Analysis (German)**	**Automotive and IP Solutions**	**Academic**
	Room Ammersee II	**Room Ammersee I**	**Room Alpsee**	**Room Chiemsee**	**Room Bodensee I**	**Room Bodensee II**	**Room Schliersee**	**Room Pilsensee**
10:30 11:00	**DSG09** Technology Overview *Cadence*	**CUS09** Automated P-Cell XOR with Instance Level Reporting *NXP*	**MS09** Verifying Analog-Mixed-Signal Designs with Cadence's Specification Driven Verification Tools *Texas Instruments*	**SVG09** Multi-Project, Multi-Site, Multi-Server: Deploying vManager Metric-Driven Signoff Platform in a Truly Global Organization *Analog Devices*	**SPB01** Enabling System-Level Design with Allegro Technologies *Cadence*	**PCB01** Enabling System-Level Design with Allegro Technologies *Cadence*	**ASIP09** ADAS System Enablement *Cadence*	**AC09** Panel: StartUp, No Money, Need for Cadence License, What to Do?
11:00 11:30		**CUS10** Common Design Migration Solution Through Universal Symbol P-Cell *NXP*	**MS10** Methodology for Spotting Floating Gate Induced Leakage Currents *Dialog Semiconductor*	**SVG10** Automated Generation of Verification Charts Using vManager CS and Highchart Library *Texas Instruments*	**SPB02** Application Driven Heterogeneous Integration *BroadPak Corporation*	**PCB02** Was Ist Neu im Schematic Entry und PCB Editor (Teil 1) *FlowCAD*	**ASIP10** ASIL-Ready Processor IP and ISO 26262 Part 11 *Cadence*	
11:30 12:00		**CUS11** Technology Overview *Cadence*	**MS11** Re-Use of a UVM Testbench in the Analog Simulation Environment *Infineon Technologies*	**SVG11** Clock Domain Crossing (CDC) and SuperLint: Two Mandatory JasperGold Apps for the Verification of IPs *STMicroelectronics*	**SPB03** Boost Automotive Co-Design Enhancement: A New SiP 17.2 Challenge *STMicroelectronics*	**PCB03** Was Ist Neu im Schematic Entry und PCB Editor (Teil 2) *FlowCAD*	**ASIP11** Scaling Up Vision and AI DSP Performance *Cadence*	**AC10** Embedded Toggle Generator to Provide Realistic Test Conditions During Test of Digital 2D-SoCs and 3D *Aristotle University of Thessaloniki*
12:00 12:30	**DSG10** Design Flow Development for Complex Designs in Advanced Technologies *Socionext*		**MS12** Supply in a Multisupply Design: VerilogAMS Simulation Strategy for Multiple Supply Domains *X-FAB Semiconductor Foundries*	**SVG12** Delivering on the Promises of Portable Stimulus *TVS*	**SPB04** Accelerate New Product Introductions with High-Performance Team Design *Cadence*	**PCB04** High-Performance Team Design *FlowCAD*	**ASIP12** Automotive Design in TSMC 16nm and 7nm *TSMC*	**AC11** High-Level Design of Finite State Machines *EXTOLL*
12:30 13:30	Lunch and Designer Expo							

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	Room Ammersee II	Room Ammersee I	Room Alpsee	Room Chiemsee	Room Bodensee I	Room Bodensee II	Room Schliersee	Room Pilsensee
12:30 13:30	Lunch and Designer Expo							
13:30 14:00	**DSG11** Integral RTL2Signoff Flow by Using Stylus for a Full Digital Flow Implementation *Texas Instruments*	**CUS12** Device Level Design Implementation Methodology *STMicroelectronics*	**MS13** Technology Overview *Cadence*	**SVG13** PSS in Real Life *Texas Instruments*	**SPB05** Allegro Solution - Adopting a RTDFA Methodology *BAE Applied Intelligence*	**PCB05** Was Bedeutet DFM für einen Leiterplattenhersteller? *AT&S*	**ASIP13** Automotive Sensor Design Enablement *Cadence*	**AC12** Cell-Aware Test: Significant Test Quality Improvement at Affordable Cost *IMEC*
14:00 14:30	**DSG12** New Optimization Strategies for High Performance CPUs Using GLOBALFOUNDRIES 22FDX Technology *GLOBALFOUNDRIES*	**CUS13** A Layout Methodology for Deep Sub-Micron Technologies *Moortec Semiconductor*	**MS14** Approaches for Improving the Failure Rate Analysis of Automotive IC Designs *Cadence*	**SVG14** Integration of vManager Metric-Driven Signoff Platform with Industry Standard DOORsNG to Address Requirement Treacebilty *NXP Semiconductors*	**SPB06** Layer Reduction and 30%+ SI Improvement Using New Via Technology *Nextgin Technology BV*	**PCB06** Welche Daten sind für einen EMS wichtig? *Zoller Elektronik AG*	**ASIP014** Efficient In-Car Communication for Safety and Convenience— Another Reason to Use Dedicated DSP Cores in Automotive IVI SoCs *Alango Technologies*	**AC13** EDA Tools and Methodologies for High-Quality Nanoelectronic Systems *Cadence*
14:30 15:00	**DSG13** Implementing a IoT Testchip and Software IP for the Arm Platform Security Architecture Using the Cadence Digital Flow *Arm*	**CUS14** Prediction of RF Synthesizer Spurs Using Substrate Noise Analysis (QRC-SNA) *S3 Semiconductors*	**MS15** Verification of Mixed-Signal HW Safety Requirements Using A Novel Mixed-Signal Fault Injection Methodology *Texas Instruments*	**SVG15** Vertical and Horizontal Code Reuse for SoC Functional Verification and Performance Analysis Stages *RnD Center «ELVEES», JSC*	**SPB07** Shorten Time to Design Your PCBs by Identifying DFx Issues Earlier in the Design Cycle *Cadence*	**PCB07** PCB DesignTrue DFM Technology *FlowCAD*	**ASIP015** Evolution of Next Generation Automotive ADAS SoC Design in 22nm FD-SOI Technology *Dream Chip Technologies*	**AC14** MEMS Design Contest — Presentations of the Winners
15:00 15:30	Coffee Break							
15:30 16:00	**DSG-Demo I** Project Stylus Introduction - Improved Productivity with CUI, Flowkit and Unified Metrics *Cadence*	**CUS-Demo I** New Technologies for Making Consumer IC Automotive Ready *Cadence*	**MS-Demo I** Power-Aware Verification of a Mixed-Signal SoC *Cadence*	**SVG16** Technology Overview *Cadence*	**SPB08** Enabling System Electrical-Thermal Design *Future Facilities*	**PCB08** Neuerungen in der OrCAD / Allegro Productivity Toolbox *FlowCAD*	**ASIP016** Innovation in Cloud-Based EDA for IoT, AI, and Semiconductor Design *Amazon Web Services*	**AC-Workshop** Agile Design Flow for Generator-Based SoC Development *Berkeley EECS*
16:00 16:30		**CUS-Demo II** Understanding the Advantages of New Virtuoso Layout Simulation-Driven Routing Techniques *Cadence*			**SPB09** Responding to Rapidly Evolving Thermal Challenges: Including but Beyond Conventional Approaches *Cadence*	**PCB09** Integrierter Analysis and Checking Workflow in Sigrity *FlowCAD*		
16:30 17:00		**CUS-Demo III** Advanced Layout Methodologies for Advanced-Node Process Technologies *Cadence*	**MS-Demo II** Improvements in Modeling Device Aging *Cadence*	**SVG-Demo** JasperGold/vManager Integration and Combined Coverage Metrics Demo *Cadence*	**SPB10** Temperature- and Geometry-Dependent Analysis of High-Speed PCB Traces *Cisco and Cadence*	**PCB10** Signalintegritätsprüfung im PCB Editor in Echtzeit *FlowCAD*		
17:00 17:30	**DSG-Demo II** Mixed-Signal Implementation Made Easy *Cadence*	**CUS-Demo IV** The Bold and the Beautiful — ADE Explorer/ Assembler Update *Cadence*	**MS-Demo III** Solving Timing Characterization Challenges for Mixed-Signal and Interface IP in Advanced Nodes *Cadence*		**SPB11** PCIe 5.0 – Addressing the Simulation, Test, and Measurement Challenges of 32Gtps *Tektronix*	**PCB11** PCB Library Management News *FlowCAD*		
17:30 18:30	Designer Expo							
18:30 20:00	Dinner and Best Presentation Awards							
20:00 23:00	Evening Event							

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Conference Agenda, Wednesday, May 9

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	Full-Flow Digital Design and Signoff	Custom	Mixed Signal and Advanced Methodologies	SoC Design and Verification	SoC Design and Verification	Signal and Power Integrity Analysis	Academic
	Room Ammersee II	Room Ammersee I	Room Alpsee	Room Chiemsee	Room Eibsee	Room Bodensee I	Room Pilsensee
07:30 08:30	Welcome Coffee and Designer Expo						
08:30 09:00	**DSG-Techtorial I** Reducing IR Drop with Automated Fixing in Tempus ECO *Cadence*	**CUS-Techtorial I** Analog IP Reuse and Process Migration: Challenges and an Innovative Methodology to Address Them *Thalia*		**SVG-Techtorial I** vAPI for Customizing vManager Verification Flows – Quickstart *Cadence*		**ICSIG-Techtorial** Signal and Power Integrity Analysis - Workshop *FlowCAD*	
09:00 09:30		**CUS-Techtorial II** Co-Simulation of Integrated Electronic and Photonic Circuits *Lumerical*	**MS-Techtorial I** How to Create an Enterprise Design and IP Management Workflow for Engineers and Business Stakeholders *Perforce*				
09:30 10:00	**DSG-Techtorial III** The Full Flow Low Power Solution – RTL to Place and Route and Signoff *Cadence*	**CUS-Techtorial III** How to Get Faster and Better Results with Spectre Accelerated Parallel Simulator *Cadence*	**MS-Techtorial II** Best Practices in Mixed-Signal Modeling and Verification *Cadence*		**SVG-Techtorial III** Portable Stimulus Standard (PSS) Techtorial *Cadence*		**AC-Techtorial I** Creating a Parameterized Layout Module with Cadence PCell Designer *Reutlingen University*
10:00 10:30		**CUS-Demo IV** Automatic Metal Filling and Trim Metal Insertion for the SADP Routing Methodology *Cadence*					
10:30 11:00	**Coffee Break and Designer Expo**						
11:00 11:30	**DSG-Techtorial III** New Innovus / PVS Hierarchical Metal Fill Flow *Cadence*	**CUS-Techtorial V** Better, Faster, Further — Updates in Virtuoso ADE Verifier *Cadence*	**MS-Techtorial III** Advanced Mixed-Signal Verification Using Xcelium Parallel Logic Simulation *Cadence*	**SVG-Techtorial II** JasperGold RTL Designer Signoff: Superlint and Clock Domain Crossing (CDC) Apps *Cadence*	**SVG-Techtorial III** Portable Stimulus Standard (PSS) Techtorial *Cadence*	**ICSIG-Techtorial** Signal and Power Integrity Analysis - Workshop *FlowCAD*	**AC-Techtorial II** Physical Implementation with ModGens *KTH Royal Institute of Technology and Cadence*
11:30 12:00	**DSG-Techtorial IV** Genus and Modus Solutions: Deep Dive Into Programmable Memory Built-In-Self-Test (PMBIST) *Cadence*						
12:00 13:00	**DSG-Techtorial VI** Think You're Smart? Try Conformal Smart LEC! *Cadence*	**CUS-Techtorial VI** Layout Dependent Effects and DFM Integration in Custom and Digital Design Flows for GF22FDX *Cadence*	**MS-Techtorial IV** Using the New Virtuoso ADE and MATLAB Integration: A Practical Guide *MathWorks and Cadence*				**AC-Techtorial III** Advancements in RFIC Design Methodology *Cadence*
13:00 14:30	**Lunch and Designer Expo**						