<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
<th>Speaker(s)</th>
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<tbody>
<tr>
<td>10:00-10:30</td>
<td>Registration Open</td>
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<tr>
<td>10:30-10:35</td>
<td>Coffee Break</td>
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<tr>
<td>10:35-11:00</td>
<td>Digital Implementations and Signoff</td>
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<td>11:00-11:30</td>
<td>Custom</td>
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<td>11:30-12:00</td>
<td>Mixed Signal</td>
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<tr>
<td>12:00-12:30</td>
<td>IP and SoC Verification</td>
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<td>12:30-13:00</td>
<td>PCB and IC Package</td>
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<tr>
<td>13:00-13:30</td>
<td>Automotive and IP Solutions</td>
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<td>13:30-14:00</td>
<td>Academic Track</td>
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<tr>
<td>14:00-14:30</td>
<td>Conference Agenda - Monday May 15</td>
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<tr>
<td>15:30-16:00</td>
<td>Networking Buffet</td>
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## Conference Agenda - Tuesday May 16

### 15:00-15:30 Coffee Break

### 15:30-16:00
- **DSG16**
  - Smooth Flow Migration from EDI to Innovus
  - S3 GROUP
- **CUS-Demo I**
  - Extracted-View-Based Power Signoff with Voltus-Fi Solution
  - Cadence
- **FV-Demo I**
  - Increase Your Debug Performance with Indago Solution’s New RTL Debug Capabilities
  - Cadence
- **SVQ08**
  - Mixed Signal Simulation: Using Spectre AMS Designer with the Xcelium Simulation Platform
  - Cadence
- **SPB08**
  - Hierarchical Circuit Diagrams for Layout and PSpice Simulation with Capture
  - Meschletana
- **PCB08**
  - Planung von Stromversorgungen auf Leiterplatten
  - FlowCAD

### 16:00-16:30
- **DSG17**
  - Library-Level Characterization of Sub-10nm Processing Nodes
  - IMEC
- **CUS-Demo II**
  - Advanced Data Mining and Analysis in Virtuoso ADE Product Suite
  - Cadence
- **SVG09**
  - Full-Speed Ethernet Implementation on the Protium S1 FPGA-Based Prototyping Platform
  - PLC2
- **SPB09**
  - Methodology for Modeling an Asynchronous Finite State Machine in PSpice
  - Infineon
- **PCB09**
  - Lösungen zur Pflege von EDA-Bibliotheken (Obsolescence and Part Management)
  - FlowCAD

### 16:30-17:00
- **DSG18**
  - To Estimate Power (at RTL Level) or Not, That Is the Question…
  - STMicroelectronics
- **CUS-Demo III**
  - Improving Productivity at Advanced Nodes Using New Layout Methodologies in ICADV 12.3
  - Cadence
- **MS-Demo II**
  - Advanced Testbench Reuse and CLIPS (Command-Line IP Selection)
  - Cadence
- **FV-Demo II**
  - Xcelium Parallel Simulator: Innovating System Simulation
  - Cadence
- **SPB10**
  - Methodology for Modeling an Asynchronous Finite State Machine in PSpice
  - Infineon
- **PCB10**
  - Planung der Testabdeckung bereits im Stromlaufplan
  - FlowCAD and XJTAG

### 17:00-17:30
- **DSG19**
  - Improving Early Power Prediction with PSpice Analog and Mixed-Signal Models
  - Cadence
- **CUS-Demo IV**
  - Bridging the Gap Between IC and PCB Design
  - Cadence
- **MS-Demo III**
  - Advanced Testbench Reuse and CLIPS (Command-Line IP Selection)
  - Cadence
- **SPB11**
  - Functional Safety Verification Solution
  - Cadence
- **PCB11**
  - Planung der Testabdeckung bereits im Stromlaufplan
  - FlowCAD and XJTAG

### 17:30-18:30 Designer Expo

### 18:30-20:00 Dinner and Best Presentation Awards

### 20:00-23:00 Evening Event
<table>
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<tr>
<th>Time</th>
<th>Session Title</th>
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<tr>
<td>07:30-08:30</td>
<td>Welcome Coffee and Registration</td>
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<tr>
<td>08:00-08:30</td>
<td>DSG-Techtorial: Advancements in Cadence Digital Implementation and Signoff Flow</td>
<td>Room Ammersee I</td>
<td>Room Ammersee I</td>
<td>Room Alpsee</td>
<td>Room Chiemsee</td>
<td>Room Bodensee I</td>
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<td>08:30-09:00</td>
<td>CUS-Techtorial I: Spectrally Updated and Performance Optimized</td>
<td>Room Ammersee I</td>
<td>Room Ammersee I</td>
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<td>09:00-09:30</td>
<td>MS-Techtorial I: Creating a UVM Environment with Scoreboard for a Mixed Signal System</td>
<td>Room Alpsee</td>
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<td>09:30-10:00</td>
<td>MS-Techtorial II: Improving EDA Reliability Verification</td>
<td>Room Alpsee</td>
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<td>10:00-10:30</td>
<td>SVG-Techtorial: Cadence/ARM-Based SoC Verification Methodology Workshop</td>
<td>Room Alpsee</td>
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<td>10:30-11:00</td>
<td>SPB-Techtorial: Sigrity Electrical Rule Checks (ERC) - Workshop</td>
<td>Room Alpsee</td>
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<td>11:00-11:30</td>
<td>AC-Techtorial: Advanced Verification Workshop – Teaching Advanced Verification Methodologies in Academia</td>
<td>Room Alpsee</td>
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<td>11:30-12:00</td>
<td>CUS-Techtorial IV: Increased Productivity Through Automatic Placement and Routing</td>
<td>Room Alpsee</td>
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<td>12:00-12:30</td>
<td>MS-Techtorial IV: Power Reference Design Flow and PFER for Inertial Sensor MEMS</td>
<td>Room Alpsee</td>
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<td>13:00-14:30</td>
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