

Conference Agenda - Monday May 15

12:00								Registration Opens							
12:00-13:30								Light Lunch Buffet							
Digital Implementation and Signoff		Custom		Mixed Signal		IP and SoC Verification		PCB and IC Package		Automotive and IP Solutions		Academic Track			
Room Ammersee II		Room Ammersee I		Room Alpesee		Room Chiemsee		Room Bodensee I		Room Schliersee		Room Pilsensee			
13:30-14:00	DSG01 25 Best HLS Coding Practices <i>NXP Semiconductors</i>	CUS01 Schematic Driven Block Isolation: No More Verification Gaps <i>NXP Semiconductors</i>	MS01 A Tool for Analog Modeling Flow Improvement Using C Functions Calls <i>Dialog Semiconductor</i>	FV01 Technology Overview <i>Cadence</i>	ICSIG01 Assembly Design Kits: An Essential Part of Chip/Package Codesign Methodology <i>Infineon</i>	ASIP01 Using a Single Core for 3GPP NB-IoT and Your Desired IoT Application - CommSolid's CSN130 is the Solution <i>CommSolid</i>	AC01 Updated Cadence 2017 Portfolio Available for European Academics via Europractice <i>Europractice</i>								
	DSG02 Design-Technology-EDA Solutions for Scaling at Single Digit Nodes with Constant Ground Rules <i>IMEC and Cadence</i>	CUS02 EAD Experience in ST Smart Power Technologies to Improve Development of IC Design <i>STMicroelectronics</i>	MS02 Mixed-Signal IP Characterization for an Internally Generated PLL Clock Using Virtuoso Liberate AMS <i>Texas Instruments</i>	FV02 Technology Overview <i>Cadence</i>	ICSIG02 An IC-Design-Centric DRC and Analysis Flow for Leadframe Packages <i>Cadence and Robert Bosch GmbH</i>	ASIP02 Real-World Wi-Fi HaLow 802.11ah Compliance Checking Environment on Virtual Platform and FPGA <i>Methods2Business</i>	AC02 Lead Institution: Leibniz Universität Hannover <i>Leibniz Universität Hannover</i>								
14:00-15:00	DSG03 Enhanced Abstract Model for Macro Blocks <i>STMicroelectronics</i>	CUS03 SenseFET Linearisation in Low-Voltage CMOS <i>University of Pretoria</i>	MS03 USB Type-C Mixed-Signal Verification <i>STMicroelectronics</i>	FV03 Technology Overview <i>Cadence</i>	ICSIG03 System Planning and Optimization Across IC, Package, and Board Using OrbitIO Interconnect Designer <i>Cadence</i>	ASIP03 Automotive DDR IP <i>Cadence</i>	AC03 Development of a Continuous Integration UVM-SystemC Framework <i>TU Braunschweig</i>								
	DSG04 Multi-Voltage Signoff with Conformal-LP Ready for ISO26262 <i>Infineon</i>	CUS04 Using Voltus-FI Solution for I/O ESD Integrity Check <i>ARM</i>	MS04 Virtuoso AMS Designer Simulation to Increase Verification Efficiency for a Digital-on-Top Project <i>Infineon</i>	FV04 Achievement of DFT Coverage Target by Combining Structural Tests and Functional Tests <i>Infineon</i>	ICSIG04 Workflow Qualification and Dependency Analysis: How to Use I/O Profiling to Protect the IT Infrastructure and Shared Storage <i>Eluxus</i>	ASIP04 IP and Driver Development in SoC/AIke Hybrid Environment <i>Robert Bosch SAS</i>	AC04 Automatic HDL Code Generation for Multisensor Digital Frontends <i>Reutlingen University</i>								
15:30-16:00								Coffee Break							
16:00-16:30	DSG05 Convert Existing Synthesis Flow to Flowkit Based on Common UI <i>NXP Semiconductors</i>	CUS05 Navigating Through the Layout Dependent Effects in Custom Analog Design <i>NXP Semiconductors</i>	MS05 Simulation of MATLAB (or Octave) with AMS by Driving the TCL Shell of IC Sim <i>Rohde & Schwarz GmbH & Co. KG</i>	FV05 Using CDC-Jitter Modelling 2-Flip-Flop Synchronizer During RTL Design Phase <i>Bosch Sensortec</i>	ICSIG05 Accelerate PCB Layout with New Real-Time Team Design Capabilities <i>Cadence</i>	ASIP05 A Wide-Range, Low-Power, Scalable JESD204A/B PHY Receiver in 28 FD-SOI <i>Cadence</i>	AC05 Teaching Microelectronics for Teenies - Internet of Things System <i>HTL-Rankweil</i>								
	DSG06 X-FAB's Reference Flow for Precise Power and IR Drop Analysis <i>X-FAB</i>	CUS06 Layout-Dependent-Effects Adoption at ST Automotive for Monitoring Electronic Control Units (ECU) <i>STMicroelectronics</i>	MS06 Design Verifications Using Cadence's Virtuoso ADE Explorer, Assembler, and Verifier <i>Texas Instruments</i>	FV06 An Efficient Flow for Complex Register Verification Using JasperGold CSR App <i>STMicroelectronics</i>	ICSIG06 Create Accurate Footprints and 3D Models Very Quickly <i>FloCAD</i>	ASIP06 Using the Cadence Tool Chain and Vision P6 Processors to Design a 22nm FD/SOI Automotive ADAS CNN SoC <i>Dream Chip Technology GmbH</i>	AC06 Teaching VHDL Design to Schoolchildren – A Scalable and Flexible FPGA Framework <i>Leibniz Universität Hannover</i>								
17:00-17:30	DSG07 Advanced Use of Voltus on a 28nm Low Power SoC Application for Automotive <i>Sonnet</i>	CUS07 Bottom Up Approach to Fix Density Issues for Base, Metal and Pre-Coloring Layers <i>IC Mask Design</i>	MS07 Mixed Signal Verification in a UVM Environment <i>Infineon</i>	FV07 A One-Fits-All Testbench Architecture <i>Dialog Semiconductor</i>	ICSIG07 Reduction of HF Emissions Obtained by Dumping the Cavity Resonances <i>STMicroelectronics</i>	ASIP07 Object Detection for Mobile and Automotive - Convolutional Neural Networks (CNNs) on Tensilica Vision DSPs <i>Leibniz Universität Hannover</i>	AC07 Undergraduate Peer-to-Peer Tutorial Authoring <i>Notre Dame University - Louaize</i>								
	DSG08 Improving Product Manufacturability with Automated DFM Optimization using Cadence LPA at 28nmFD/SOI <i>STMicroelectronics</i>	CUS08 Modern Search Techniques for Layout Creation <i>STMicroelectronics</i>	MS08 Full-Chip Software and IC Co-Verification Methodology Using SystemVerilog Real Number Models <i>LG Electronics Finland Lab Oy</i>	FV08 MOV Automation: Self Coverage Filling Test Benches <i>Infineon</i>		ASIP08 Cost-Effective Automotive Ethernet Compliance Testing <i>Cadence</i>	AC08 Simulation-Driven Impact Analysis of Layout Parasitics in AMS Circuits <i>IMMS</i>								
18:00-20:00								Networking Buffet / Designer Expo							

Conference Agenda - Tuesday May 16

Welcome Coffee and Registration									
Keynotes									
Davide Santo: Autonomous Architect – ADAS PL, NXP									
Tom Beckley: Senior Vice President and General Manager, Custom IC & PCB Group, Cadence									
Coffee Break									
	Digital Implementation and Signoff	Custom	Mixed Signal	IP and SoC Verification	Software and System Verification	PCB Design and Analysis	PCB Design and Analyse (German/Deutsch)	Automotive and IP Solutions	Academic
	Room Ammersee II	Room Ammersee I	Room Alppsee	Room Chiemsee	Room Eibsee	Room Bodensee I	Room Bodensee II	Room Schliersee	Room Pilsensee
07:30-08:45									
08:45-10:00									
10:00-10:30									
10:30-11:00	DSG09 Technology Overview Cadence	CUS09 Cadence Schematic P-Cell: Not Something Exotic but Mandatory Technology for Everyday Tasks NXP Semiconductors	MS09 Technology Overview Cadence	FV09 Dynamic Reseeding for Power Aware Simulation Speedup Infineon	SVG01 Cadence VSP – Control Process Application Implemented on the Zynq-7000 Virtual Platform Ruhr University Bochum	SPB01 Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces Cadence	PCB01 Cadence PCB Update: Was ist neu im Schematic Entry und PCB Editor - Teil I	ASIP09 Automotive Electronics Redefined Cadence	AC09 Panel: From Academic Idea to Commercial IP Europacore Software Services, EXTOLL GmbH RagYCS, Cadence
11:00-11:30	DSG10 Technology Overview Cadence	CUS10 Schematic and Symbol PCell Development with Cadence PCell Designer Robert Bosch GmbH	MS10 Technology Overview Cadence	FV10 Automated UVM Register Field Probe Dialog Semiconductor	SVG02 Rapid Prototyping of Perspec Test Cases on Fast Virtual Multi-Cluster Platforms Cadence	SPB02 Optimizing Connector-PCB Transitions with Integrated Mechanical-Electrical Analysis Cadence	PCB02 Cadence PCB Update: Was ist neu im Schematic Entry und PCB Editor - Teil II FlowCAD	ASIP10 Advanced Platform for Highly Automated Driving Renesas Electronics Europe	AC10 Panel: From Academic Idea to Commercial IP Europacore Software Services, EXTOLL GmbH RagYCS, Cadence
11:30-12:00	DSG11 Reference Physical Implementation Challenges of a High Performance ARM Mali GPU ARM	CUS11 Technology Overview Cadence	MS11 A Concept for Expanding a UVM Testbench to the Analog-Centric Toplevel Bosch Sensortec	FV11 Deploying Jasper and Simulation Mutually-Exclusive using JasperGold's ProofCore Technology Infineon	SVG03 Stochastic Profiling of Embedded Software in Mixed-Mode IC Simulation Melsis	SPB03 What's New in Sigrity 2017 and What's Coming Soon Cadence	PCB03 Erfahrungen beim Design von komplexen High-Power Baugruppen Semikron	ASIP11 MIMO Radar Signal Processing on Tensilica DSPs Cadence	AC11 Hardware Enhanced Security for Documents Universität Tübingen
12:00-12:30	DSG12 Advanced ARM Cortex-A CPU Power and Frequency Optimization ARM	CUS12 Technology Overview Cadence	MS12 Developing a Top-Down Design and Shortening Verification Environment for Mixed-Signal Chip Cadence	FV12 Improving Verification Quality and Shortening Debugging Time Using JasperGold Control and Status Register (CSR) Verification App Renesas Electronics Europe	SVG04 A Pattern Library for the Generation of Portable Use Cases Using Perspec System Verifier Ruhr University Bochum	SPB04 Team-Based Power-Integrity Analysis to Accelerate Design Cycles Cadence	PCB04 Definition und Designregeln für starre/flexible Leiterplatten im OrCAD / Allegro PCB Editor FlowCAD	ASIP12 A New Computer Vision Processor Chip Design for Automotive ADAS CNN Applications in 22nm FDSOI Dream Chip Technology GmbH	AC12 SKILL Application Manager (SAM) - Simplify Your Software Development in Virtuoso Reutlingen University
12:30-13:30	Lunch / Designer Expo / Canvas Conversation								
13:30-14:00	DSG13 RTL FMBIST on an ADI 65nm 3.8 Million Instance Design Analog Devices	CUS13 Cadence Virtuoso ADE Product Suite - An Automotive Smart Power TR&D Joint Project Walk-Through STMicroelectronics	MS13 Method for 1 to 1 Mapping an Analog Topology to a SystemVerilog Code Infineon	FV13 UVM Based SoC Bus Infrastructure TB Generator CommSolid	SVG05 Modelling Primitives for Approximately Timed SystemCTLM Models Cadence	SPB05 OrCAD Capture Cloud: Make OrCAD & Arrow the Easy Choice for New Start-Up and Maker Customers Arrow	PCB05 Unterschiede der Basismaterialien für den Lageraufbau einer Leiterplatte Isola	ASIP13 Scalable Neural Network Processors for Embeddable Applications Cadence	AC13 Network-on-Chip Design for System-on-Chip with Reconfigurable Components Saint-Petersburg State University of Aerospace Instrumentation
14:00-14:30	DSG14 Image Sensor Design and Verification Challenges: ADC Design Aspects and Transition to UVM x2v-AnalFocus	CUS14 How to Speed Up High-Fanout P/G Routing Closure on Large Automotive Design for SmartPower Technology STMicroelectronics	MS014 A Methodology for Analog Fault Injection at Primitive Level Melsis	FV14 Automating Requirements Verification Loop Using Cadence vPlanner/Manager Texas Instruments	SVG06 TCL and Scripting: How to Get the Most Out of HLS Verint Solutions	SPB06 Raspberry Pi Zero W: Solving the Complexities of Cost Sensitive Miniaturisation with Cadence Design Tools Raspberry Pi	PCB06 Hintergrundinformationen zur Leiterplattenfertigung und Designregeln Würth Elektronik	ASIP14 Functional Safety and Reliability Methodologies for Automotive Applications Cadence	AC14 Enabling Energy Transparency to Tackle the IoT Energy Challenge Bristol University
14:30-15:00	DSG15 16nm Design Experiences Renesas Electronics Europe	CUS15 Stress Reduction in Drivers with Complex PCells X-FAB	MS15 AMS IP Requirement Driven Development Flow: Best Practice of AMS Verification Infineon	FV15 UVM-ML Message From the Trenches Verilab GmbH	SVG07 Stratus HLS Interconnect IP for Subsystem Analysis and Implementation Cadence	SPB07 Streamline ECAD-MCAD Co-Design Leveraging Allegro/OrCAD Interactive 3D Canvas Cadence	PCB07 Customer Miniaturization Wintersonn		AC15 Cadence Academic Network Design Contests: Poster Session
15:00-15:30	Coffee Break								

Conference Agenda - Tuesday May 16

Coffee Break										
	Digital Implementation and Signoff	Custom	Mixed Signal	IP and SoC Verification	Software and System Verification	PCB Design and Analysis	PCB Design und Analyse (German/Deutsch)	Automotive and IP Solutions	PCB Design and Analysis	Academic
	Room Ammersee II	Room Ammersee I	Room Alpssee	Room Chiemsee	Room Eibsee	Room Bodensee I	Room Bodensee II	Room Schliersee	Room Pfäensee	Room Pfäensee
15:00-15:30										
15:30-16:00	DSG16 Smooth Flow Migration from EDI to Innovus S3 GROUP	CUS-Demo I Extracted-View-Based Power Signoff with Voltus-FI-L Solution Cadence	MS-Demo I Mixed Signal Simulation: Using Spectre AMS Designer with the Xcellium Simulation Platform Cadence	FV-Demo I Increase Your Debug Performance with Indago Solution's New RTL Debug Capabilities Cadence	SVG08 Choosing the Right Models for Verification and Software Development ARM	SPB08 Hierarchical Circuit Diagrams for Layout Verification and PSpice Simulation with Capture Mischelana	PCB08 Planung von Stromversorgungen auf Leiterplatten FlowCAD	ASIP15 User Experiences with IFS5 Infineon		AC16 European Training Network H2020 RESCUE - Interdependent Challenges of Reliability, Security and Quality in Nanoelectronic Systems Design TU Delft
16:00-16:30	DSG17 Library-Level Characterization of Sub-10nm Processing Nodes IMEC	CUS-Demo II Advanced Data Mining and Analysis in Virtuoso ADE Product Suite Cadence			SVG09 Full-Speed Ethernet Implementation on the Protonium S1 FPGA-Based Prototyping Platform PLC2	SPB09 Pspice: Expanded Applications (SLPS with Mathworks, AA Simulation for all Circuits) FlowCAD	PCB09 Integrierte thermische Simulation von Leiterplatten im OrcAD/Allegro CAD-Flow FlowCAD	ASIP16 Multi-Fabric ECU and Sensor Design Enablement for the ADAS/AV Automotive Age Cadence		
16:30-17:00	DSG18 To Estimate Power (at RTL Level) or Not, That Is the Question..... STMicroelectronics	CUS-Demo III Improving Productivity at Advanced Nodes Using New Layout Methodologies in ICADV 12.3 Cadence	MS-Demo II Advanced Testbenches Reuse and CLIPS (Command-Line IP Selection) Cadence	FV-Demo II Xcellium Parallel Simulator: Innovating System Simulation Cadence	SVG-Demo Protobus: FPGA-Based Prototyping Made Easy - Reduce Bring-Up Time from Months to Weeks! Cadence	SPB10 Methodology for Modeling an Asynchronous Finite State Machine in PSpice Infineon	PCB10 Lösungen zur Pflege von EDA-Bibliotheken (Obsolescence and Part Management) FlowCAD	ASIP17 Functional Safety Verification Solution Cadence		SPB-Demo PCB Team Design (Live Demo of Two Layers Collaborating) and Productivity Toolbox FlowCAD
17:00-17:30	DSG19 Improving Early Power Prediction with RTL Stimuli Using Joules NXP Semiconductors	CUS-Demo IV Bridging the Gap Between IC and Package/Module Cadence				SPB11 Computer Modeling and Simulation of Photovoltaic Panels Using PSpice Technical University of Sofia	PCB11 Planung der Testabdeckung bereits im Stromlaufplan FlowCAD and XITAG			
17:30-18:30	Designer Expo									
18:30-20:00	Dinner and Best Presentation Awards									
20:00-23:00	Evening Event									

Conference Agenda - Wednesday May 17

07:30-08:30 Welcome Coffee and Registration						
	Digital Implementation and Signoff	Custom	Mixed Signal	System Design and Verification	PCB and IC Package Analysis	Academic
	Room Ammersee II	Room Ammersee I	Room Alpsee	Room Chiemsee	Room Bodensee I	Room Pilsensee
08:30-09:00	DSG-Techtorial Advancements in Cadence Digital Implementation and Signoff Flow – Technical Deep Dive Cadence	CUS-Techtorial I Spectre Technology Update and Performance Optimization Cadence	MS-Techtorial I Creating a UVM Environment with Scoreboard for a Mixed-Signal Image Cadence	SVG-Techtorial Cadence/ARM-Based SoC Verification Methodology Workshop Cadence	SPB-Techtorial Signity Electrical Rule Checks (ERC) - Workshop FlowCAD and Cadence	AC-Techtorial Advanced Verification Workshop – Teaching Advanced Verification Methodologies in Academia Cadence, University of Bristol, Extoll GmbH
09:00-09:30			MS-Techtorial II Improving SoC Robustness and Yield with AMS Designer Reliability Verification Cadence			
09:30-10:00			MS-Techtorial III SystemVerilog "Ecmnet" Nettype Usage and its Application to Voltage Doubler Modeling Cadence			
10:00-10:30			CUS-Techtorial II An Integrated Methodology for 3D EM Modeling of On-Chip Structures Cadence			
10:30-11:00 Coffee Break / Designer Expo						
11:00-11:30	DSG-Techtorial Advancements in Cadence Digital Implementation and Signoff Flow – Technical Deep Dive Cadence	CUS-Techtorial III Memory Characterization with Liberate MX Cadence	MS-Techtorial IV Da Capo, Maestro) Interactive Techtorial on Virtuoso ADE Explorer, Assemble, and Verifier Cadence	SVG-Techtorial Cadence/ARM-Based SoC Verification Methodology Workshop Cadence	SPB-Techtorial Signity Electrical Rule Checks (ERC) - Workshop FlowCAD and Cadence	AC-Techtorial Advanced Verification Workshop – Teaching Advanced Verification Methodologies in Academia Cadence, University of Bristol, Extoll GmbH
11:30-12:00		CUS-Techtorial IV Increased Layout Productivity Through Automatic Placement and Routing Cadence				
12:00-12:30		CUS-Techtorial V Pioneer Reference Design Flow and PDK for Inertial Sensor MEMS Coventor				
12:30-13:00		CUS-Techtorial VI Schematic-Driven Simulation and Layout of Complex Photonic ICs Lumental Solutions				
13:00-14:30 Lunch / Designer Expo						