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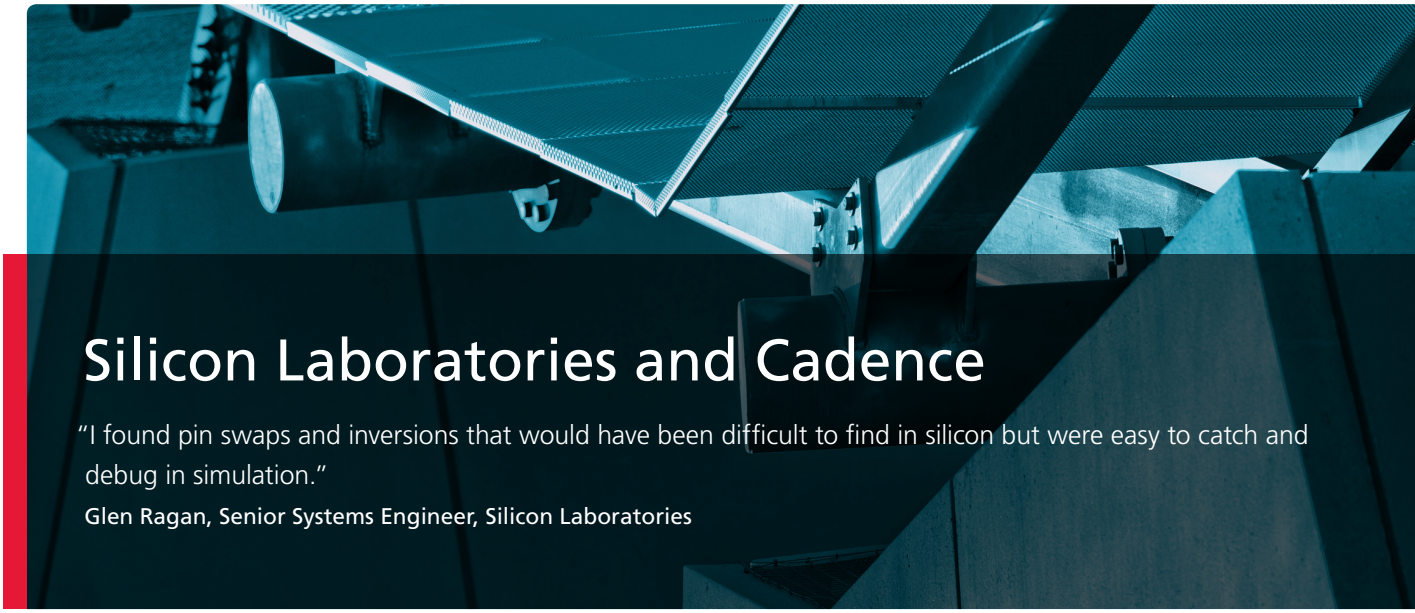

Silicon Laboratories and Cadence

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Glen Ragan, Senior Systems Engineer, Silicon Laboratories

The Customer

Founded in 1996 and headquartered in Austin, Texas, Silicon Laboratories is an industry leader in high-performance, analog-intensive, mixed-signal integrated circuits (ICs). The company creates innovative products for the microcontroller, audio-video, modem, and subscriber line markets.

The Challenge

Within the Broadcast Group of Silicon Labs, which develops FM and TV tuners, a focus on analog design means that the analog design teams verify the blocks while the digital verification team integrates the digital and analog content at the chip level. Verifying the full chip with Spice (or even FastSpice) models would be prohibitively slow.

"Even if full chip analog simulation could have been run, it would have taken 9-10 days," says Jeff Alderson, Senior Design Engineer at Silicon Labs. "Using wreal models our regressions finish in around four hours."

The Solution

Performance was a key consideration for Silicon Labs when investigating the use of digital/mixed-signal (DMS) technology. The DMS Option for Cadence® Incisive® Enterprise Simulator takes advantage of the wreal construct in Verilog-AMS to seamlessly connect real value models (RVMs) to the digital content. Because RVMs are event based, they are evaluated in the digital simulator to achieve much faster performance.

Business Challenge

- Fast time to market for mixed-signal ICs, without compromising performance

Design Challenge

- Full-chip verification with Spice or FastSpice was too slow

Cadence Solution

- Incisive Enterprise Simulator

Results

- Improved performance and productivity with wreal construct in Verilog-AMS, which seamlessly connects real value models to digital content
- Achieved higher-quality product with accurate modeling, which simulates real chip performance

"Because of the large amount of analog content in our designs, we must run full chip verifications with accurate analog models," says Jayanth Shreedhara, CAD Engineer at Silicon Labs. Silicon Labs uses RVMs to abstract the function of the analog content.

"We develop the models to represent the accuracy we need. For the analog blocks that are part of a feedback loop from the digital side, those models are modeled accurately enough to simulate actual chip performance," Jeff Alderson adds.

By modeling ADCs, analog multiplexers, multipliers, sigma delta converters, filters, and other analog devices using RVMs, they were able to keep the simulation of analog intensive modules in the digital domain, which runs much faster than the analog solver.

Why not just use Verilog behavioral models to represent the analog content? Connectivity checking between the analog and digital parts of the design is critical since the two domains are usually created and verified separately. The checking is often done by hand by having several layers of people manually check the connection of each pin to verify it is correct.

Verilog-D behavioral models may be written to represent the functionality, but Verilog-D is limited in its ability to pass a 64-bit real value across a port. There are also limitations with vectors of real values and resolution problems when connecting multiple real value ports. Using the Verilog-AMS wreal construct (which allows a real value to be assigned to a single-bit wire), along with the DMS Option to Incisive Enterprise Simulator, resolves those issues.

Silicon Labs used the wreal construct along with RVMs to accurately and easily create its mixed-signal environment. And since the RVMs matched pin to pin with the Spice models, the Silicon Labs team was able to find numerous quality problems using simulation versus having to conduct multi-day design reviews where the designers go pin by pin to manually validate connectivity and polarity.

"I found pin swaps and inversions that would have been difficult to find in silicon but were easy to catch and debug in simulation," says Glen Ragan, Senior Systems Engineer at Silicon Labs.

He adds that "having wreals react to digital inputs and vice versa was simple to construct versus having to interface to electricals. This made critical digital to analog to digital loops fairly simple to validate."

With the ease and speed of creating RVMs, the digital verification effort has been able to start sooner.

"We can create RVMs very quickly and don't have to wait for the final Spice models" Alderson says. "The digital verification team has been able to take on more top-level verification responsibility because models have been quick to develop. Instead of using just simple buffers to represent the analog, the wreal models were more accurate and provided more checking. In other words, the use of wreal models in our mixed-signal verification flow, significantly improved our overall verification productivity. Overall, it reduced our regression runtime from weeks to hours with a much better quality product."

Summary and Future Plans

Silicon Labs has been able to take advantage of the performance, quality, and productivity improvements offered through the use of wreal and RVMs. The company looks forward to using more of the advanced capabilities such as arrays of wreals and wreal resolution in their next project.

Both Ragan and Alderson enthusiastically agreed that, "The new features offered with the Incisive Enterprise Simulator DMS Option will allow us to further improve our verification environment."