



University Program Software Selection

Americas University Program 2010

Custom Integrated Circuits Bundle

The Custom IC Bundle Software Reference List:

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Design Environment		
Virtuoso [®] AMS Designer Environment	70000	IC 6.1
Virtuoso [®] Analog Design Environment - XL	95210	IC 6.1
Virtuoso [®] Analog Design Environment - GXL	95220	IC 6.1
Design Entry		
Cadence [®] SKILL Development Environment	900	IC 6.1
Virtuoso [®] Schematic VHDL Interface	21060	IC 6.1
Virtuoso [®] Schematic Editor Verilog ^R Interface	21400	IC 6.1
Virtuoso [®] Schematic Editor - XL	95115	IC 6.1
Virtuoso [®] Analog Oasis Run-Time Option	32100	IC 6.1
Layout		
Virtuoso [®] Layout Suite - GXL ¹	95321	ICS 6.1.2
Cadence [®] Chip Assembly Router ²	3300	IC 6.1
RF System-In-Package (SIP)³		
Cadence [®] SiP RF Architect - XL	SIP410	SPB 16.3
Cadence [®] SiP Layout – XL	SIP225	SPB 16.3

¹ includes CIF reader/writer and Virtuoso Stream Interface

² includes GDSII/EDIF and LEF/DEF interfaces

³ must be installed with Virtuoso



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<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Physical Verification		
Dracula [®] Graphical User Interface	365	IC 6.1
Dracula [®] Physical Verification and Extractor Suite	70520	IC 6.1
Diva [®] Physical Verification and Extractor Suite	71520	IC 6.1
Assura [™] Design Rule Checker	72110	Assura 4.1
Assura [™] Layout vs. Schematic Verifier	72120	Assura 4.1
Virtuoso [®] QRC Extraction - L	QRCX100	EXT 9.1
Virtuoso [®] QRC Extraction - XL	QRCX300	EXT 9.1
Virtuoso [®] Advanced Analysis GXL option	QRCX310	EXT 9.1
Assura [™] Graphical User Interface Option	72140	Assura 4.1
Assura [™] Multiprocessor Option	72150	Assura 4.1
Pcell Generator	PASPCG	PAS 3.1
Graphical Technology Editor	PASGTE	PAS 3.1
Generator for Assura [™] compatible verification decks	PASASG	PAS 3.1
Generator for Diva [®] compatible verification decks	PASDIG	PAS 3.1
Generator for Dracula [®] compatible verification decks	PASDRG	PAS 3.1
Error Cell Generator	PASECG	PAS 3.1
Circuit Simulation		
Virtuoso [®] Schematic Editor HSPICE Interface ¹	276	IC 6.1
Virtuoso [®] Analog Design Environment - GXL	95220	IC 6.1
Virtuoso [®] Spectre [®] Circuit Simulator	38500	MMSIM 7.2
Virtuoso [®] UltraSim Full-chip Simulator	33500	MMSIM 7.2
Virtuoso [®] Spectre [®] RF Simulation Option for 38500	38520	MMSIM 7.2
Virtuoso [®] Analog HSPICE Interface Option ¹	32760	IC 6.1
AMS Designer with Flexible Analog Simulation	70020	IUS 8.2
Virtuoso [®] Multi-mode Simulation with AP Simulator	90003	MMSIM 7.2
Interfaces		
Virtuoso [®] EDIF 200 Reader	940	IC 6.1
Virtuoso [®] EDIF 200 Writer	945	IC 6.1
Cadence [®] Design Framework Integrator's Toolkit	12141	IC 6.1

¹ requires additional licenses that must be obtained from Synopsys



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Digital Integrated Circuits Bundle

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<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Place & Route and Timing		
Virtuoso [®] Layout Suite - GXL	95321	ICS 6.1.2
Cadence [®] Chip Assembly Router	3300	IC 6.1
Physical Verification		
Dracula [®] Physical Verification and Extractor Suite	70520	IC 6.1
Design for Manufacturing		
Virtuoso [®] QRC Extraction - L	QRCX100	EXT 9.1
VoltageStorm (transistor)	VST1	ANLS 6.2
Encounter Power System - L	EPS100	ETS 9.1
Signal Integrity		
Encounter [™] Timing System - XL	FE725	ETS 9.1
Pacific Static Noise Analyzer for Custom Digital ICs	CM00100	PACIFIC 6.1
Encounter [™] Timing System - L	FE625	ETS 9.1
Encounter [™] Library Characterizer- XL	ELC200	ETS 9.1
Silicon Virtual Prototyping		
Encounter [™] Digital Implementation System - XL	EDS200	EDI 9.1
Encounter [™] Low Power GXL Option	EDS10	EDI 9.1
Encounter [™] Advanced Node GXL option	EDS30	EDI 9.1
Test		
Architect Advanced Option to RC	ET021	ET 9.1
Encounter [™] True Time Test Advanced	ET023	ET 9.1
Encounter [™] Diagnostics Engine - XL	ET009	ET 9.1
Digital System-In-Product (SiP)¹		
Cadence [®] SiP Digital Architect - GXL	SIP125	SPB 16.3
Cadence [®] SiP Digital SI - XL	SIP215	SPB 16.3
Cadence [®] Chip Integration Option	SIP625	SPB 16.3

¹ must be installed with Encounter



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The Digital IC Bundle Software Reference List, continued

Formal Verification

Encounter TM Conformal - GXL	CFM300	CONFRML 9.1
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Synthesis

Encounter TM RTL Compiler - XL	RC200	RC 9.1
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Encounter TM RTL Compiler - GXL option	RC300	RC 9.1
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Chip Planning

Cadence [®] InCyte Chip Estimator L	CPS100	CICE3.7
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Cadence [®] InCyte Chip Estimator XL	CPS200	CICE3.7
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Verification Bundle

The Verification Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Functional Verification		
Incisive Enterprise Simulator - L	29610	IUS 8.2
Cadence [®] Simulation Analysis Environment (SimVision)	25010	IUS 8.2
Verifault – XL Simulator	26500	IUS 8.2
Incisive [™] Enterprise Simulator	29651	IES 8.2
Enterprise Simulator - XL Interface for MTI	29661	IES 8.2
Enterprise Simulator - XL Interface for VCS	29671	IES 8.2
Incisive [™] Formal Verifier	23560	IFV 8.2
Incisive [™] Software Extensions	ISX100	INCISV 9.2
Virtuoso [®] AMS Designer Verification Option	70030	INCISV 9.2
Verification Process Automation		
Incisive [™] Enterprise Manager	EMG100	EMGR 8.2
Pre-verified, Re-usable Verification IP Components		
AMBA AHB protocol	UVC100	UVCAMBA 2.5
USB protocol	UVC101	UVCUSB 2.6
PCI Express End Point protocol	UVC102	UVCPCIE 2.3
PCI Express Root Complex protocol	UVC103	UVCPCIE 2.3
PCI 2.2/2.3 protocol	EVC1004	EVCPCI 2.2
Ethernet protocol	EVC1006	EVCETH 2.2
AMBA AXI protocol	UVC107	UVCAMBA 2.5
Incisive [™] VIP Portfolio	VIP100	VIPP 9.2



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Silicon-Package-Board Bundle

The Packaging & Board Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
PCB Design and Layout		
Allegro [®] PCB Librarian - XL	PX3500	SPB 16.3
Allegro [®] PCB Design HDL - XL	PX3700	SPB 16.3
Allegro [®] PCB Design CIS - XL	PX3710	SPB 16.3
PCB High-Speed Analysis		
Allegro [®] PCB SI - XL	PX3100	SPB 16.3
IC Packaging		
Cadence [®] SiP Layout – XL	SIP225	SPB 16.3
Simulation		
Allegro [®] AMS Simulator ¹	PS2200	SPB 16.3

¹ superset of Pspice and Advanced Analysis Option