Encounter Digital Implementation System

The fastest, most predictable path to power, performance, and area realization

Cadence® Encounter® Digital Implementation (EDI) System provides the most effective methodology to maximize power, performance, and area for high-performance, giga-scale designs. Integration with the Virtuoso® custom design environment ensures seamless data transfer and increases productivity for mixed-signal designs. EDI System also supports advanced 20nm process technologies and system-in-package/3D-IC design. With these capabilities, EDI System delivers the most comprehensive solution for physical implementation of today's most demanding designs.

Encounter Digital Implementation System

Based on design intent, abstraction, and convergence, Encounter Digital Implementation (EDI) System gives you an early, accurate view of design feasibility and allows you to progress immediately to full-scale implementation and final signoff for large-scale, complex designs—without ever leaving the solution environment.

EDI System combines early and rapid design exploration and accurate chip feasibility analysis (using unique and patented abstraction technology); automated floorplan synthesis; clock tree and clock mesh synthesis; advanced nanometer routing; full-chip virtual prototyping; and full-chip digital implementation and signoff in a single environment. EDI System supports the implementation of high-performance designs, giga-scale designs, and mixed-signal designs, and it addresses the design scale, complexity, and manufacturing requirements of 28/20nm advanced node designs, including double-patterning requirements. It also offers integrated statistical-based analysis and optimization, as well as 3D-IC and silicon-in-package technology. With these capabilities, EDI System helps you achieve the best power, performance, and area within the most aggressive project timelines.

Benefits

Predictability and convergence

- Combines full-chip implementation with in-design signoff analysis in a single environment
- Enables design exploration and accurate chip feasibility analysis, including automated floorplan synthesis and ranking, as well as hierarchical budgeting and planning for convergent hierarchical implementation results
- New GigaOpt and CCOpt engines deliver better power, performance, and area results for high-performance designs, allowing block implementation to meet and exceed aggressive goals
- Achieves faster, more convergent timing closure by using same extraction engine during in-design and signoff
- Supports comprehensive multi-mode/multi-corner analysis and optimization in all steps throughout the flow
- Supports location-based on-chip-variation technologies and the latest methodologies for statistical timing and leakage analysis and optimization

Productivity and faster time to market

- Supports hierarchical methodologies including bottom-up block-based flows, top-down black-box flows, and hybrid flows with partitioning and time budgeting
- GigaFlex technology adapts to growing capacity requirements while still retaining the relevant timing, placement, and congestion information to accurately plan and implement giga-scale designs

- FlexModels provide up to 90% netlist compression and an optimized interface for accurate design exploration and planning, resulting in faster turnaround time and one-pass implementation handoff
- FlexILMs and FlexViews enable concurrent top- and block-level implementation and closure for hierarchical designs; more transparent hierarchical abstraction; and fewer iterations during top-level optimization and assembly
- Supports a constraint-driven mixed-signal environment through the OpenAccess database, allowing for concurrent custom/digital design methodologies with smoother transitions between Virtuoso and Encounter environments
- Performs fast and accurate optimization and analysis in the flat physical implementation flow by leveraging the new multi-CPU/multi-threaded–enabled Advanced Analysis Engine for single-step timing and signal integrity delay calculation
- Delivers signoff-driven analysis during design implementation including multi-mode/multi-corner signoff ECO, as well as intuitive visual features for global timing, power, signal integrity, and clock tree diagnostics

Scalability in performance

- Delivers industry-leading performance and capacity for large, complex chips
- Offers a complete, end-to-end, multi-core parallel processing backplane and infrastructure
- Provides best-in-class, efficient multi-corner functionality to significantly improve turnaround time

Differentiated product development with lower production costs

- Includes comprehensive support for 28/20nm designs to handle design scale and complexity as well as new DFM requirements

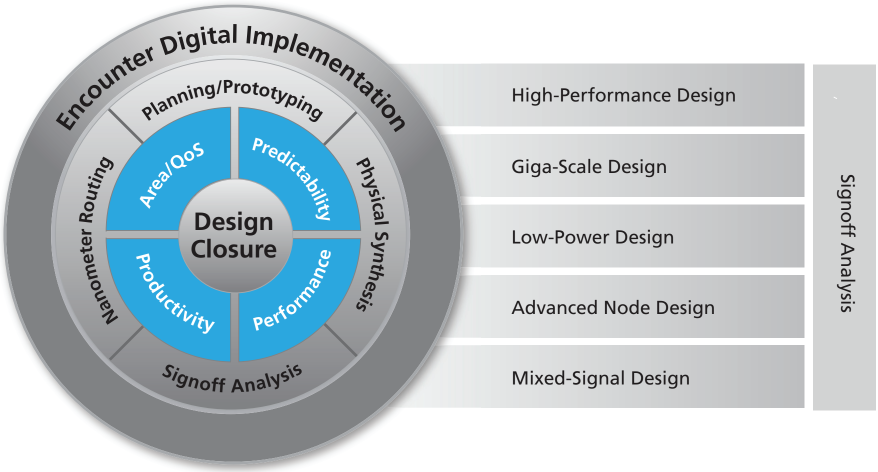

Figure 1: Encounter Digital Implementation System delivers a comprehensive solution

- Supports 20nm double-patterning physical implementation and signoff requirements, from placement and routing to timing, power, and physical signoff
- Enables concurrent chip/package co-design and optimization with integrated capabilities such as automatic area and peripheral I/O placement and flip-chip RDL routing
- Allows floorplanning, implementation, and analysis of 3D stacked-die designs with through-silicon-via (TSV) connectivity for optimization of heterogeneous processes/dies, ensuring fewer iterations and faster convergence with in-design 3D-IC signoff extraction and timing/power analysis across multiple dies

High-Performance Design

At smaller process geometries, designing an SoC for the next smartphone, tablet computer, gaming console, or high-end wireless device requires implementing several complex subsystems (including high-performance CPU, GPU, DSP, and video compute engines) and high-speed interconnect fabric. These designs are difficult to implement in silicon, especially with the aggressive performance targets at very low-power budgets. Customers in the consumer, mobile computing, wireless, and networking markets are moving ahead with 32/28nm and 22/20nm process nodes while pushing the envelope on power, performance, and area (PPA) metrics.

Several new underlying technologies in EDI System 11—such as the GigaOpt optimization engine and clock concurrent optimization (CCOpt)—help meet such overwhelming demands on PPA targets at advanced nodes. These capabilities enable SoC implementers to differentiate their products without significantly escalating the costs of getting leading-edge designs to market.

CCOpt and GigaOpt

Clocking is the backbone of modern SoC designs, and clock tree synthesis (CTS) is an essential capability that distributes clock signals to the data registers. Inherent to the task of designing a high-performance SoC is implementing the design's complex clock system. In today's SoC physical design flows, CTS is separate from physical optimization. While this approach has generally worked down to the 40nm node, it is now breaking down because on-chip variation, low-power demands, and complexity are causing a significant "timing gap" between the ideal clocks used pre-CTS and the propagated clocks used post-CTS.

Cadence clock concurrent optimization (CCOpt) is a new approach to timing optimization that holistically addresses this timing gap. CCOpt brings the realm of physical optimization into CTS, and is the only tool that optimizes the clock insertion as well as logic delays simultaneously, instead of doing them separately. In addition to CTS, it encompasses timing-driven placement, incremental physical optimization, physical clock gating, and post-clock tree optimization. Observed results have included clock-tree power reductions of 30%, clock-tree area reductions of 30%, and chip performance improvements up to 100MHz for a GHz+ design. No manual tweaking of clock trees and skew balancing is necessary. CCOpt performs concurrent useful-skew and datapath optimization, as well as time borrowing for faster timing closure, leading to significant productivity improvements. Additional benefits include up to 30% reduction in IR drop (because registers and RAMs are triggered at different times) and a skew profile that reduces peak current by up to 40% without any impact on timing.

EDI System 11 also includes a new engine called GigaOpt, which is a fast and scalable optimization engine that provides better quality of results (QoR) with faster runtime. Initial results show that GigaOpt in EDI System 11 delivers approximately 3.5x runtime speed-up compared to the EDI System 10 post-route flow, and it also provides better timing QoR. GigaOpt is available for post-route in EDI System 11. However, Cadence R&D plans to make GigaOpt the default optimization engine throughout the entire implementation flow, from pre-route optimization to post-route closure.

Bringing all these technologies together, Cadence has jointly developed state-of-the-art RTL-to-GDSII implementation reference methodologies with industry-leading silicon IP vendors for high-performance microprocessor-based designs. These reference methodologies were developed to help you achieve optimal PPA with reduced effort and increased productivity. They also feature capabilities such as power shutoff, advanced floorplanning, CCOpt, and the new GigaOpt engine.

Power management

EDI System is an integral part of the Cadence Low-Power Solution. This comprehensive methodology supports the Common Power Format (CPF), which captures all power-specific design intent, from power-aware design planning to final implementation and through to signoff. The underlying infrastructure of EDI System simplifies the implementation of low-power designs because it is multi-power-domain–aware across the flow. Floorplanning, placement, clock tree synthesis, optimization, routing, analysis, and all other steps in the design flow comprehend and optimize power across all domains simultaneously.

Native integration of complete multi-supply voltage (MSV) management enables automatic placement of level shifters with all power connections completed automatically. This allows you to implement designs that employ advanced power reduction techniques such as power shutoff (PSO), MSV, dynamic voltage/frequency scaling (DVFS), substrate biasing, and many more. A powerful engine optimizes the power delivery network using early rail analysis for concurrent chip and package power modeling, ensuring convergence for the design's power network.

Today's low-power designs also have to work seamlessly in a hierarchical flow and leverage the abstraction advantages of integrating IP models from other sources. To ensure a seamless hierarchical flow and IP integration, Cadence offers hierarchical low-power macro modeling of black boxes. This helps you take advantage of hierarchical abstraction as well as the scalability of integrating IP in low-power designs.

Advanced global debug and diagnostics

Debug and diagnosis challenges often come late in the design cycle, along the critical path to final tapeout. EDI System provides timing, power, signal integrity (SI), and clock debug and diagnostics capabilities that allow you to quickly locate and visualize interdependent timing, clock, SI delay and glitch, and power issues, and then quickly resolve them using powerful "what-if" analysis techniques. These results can be immediately implemented in physical design

Giga-Scale Design

With design sizes increasing toward the 100+ million instance range, it is critical that the design implementation system can handle designs of such scale. In EDI System 11, GigaFlex technology greatly expands the system's capacity to handle giga-scale designs of 100M instances or more, helping you achieve full-chip design prototyping goals; uncover potential issues earlier; and, meet timing and SI requirements on multiple extraction corners and up to 100 multi-mode/multi-corner (MMMC) timing views, allowing you to produce the most optimal design floorplan. Concurrent top- and block-level hierarchical implementation reduces iterations and total design cycle time for giga-scale designs. In addition, MMMC signoff engineering change order (ECO) capability leverages a multi-CPU and multi-threaded backplane with fast and accurate extraction to enable fully automated, physically aware, high-capacity timing ECOs applicable at the full-chip level.

Early design exploration

Today's physical design teams start physical implementation and design planning very early in the design cycle—with early and multiple versions of the design netlist—to determine design feasibility. EDI System closes the gap between architecture and implementation, addressing questions such as whether the design can be implemented in the required area, and if it will operate at the desired speed.

- GigaFlex technology extends patented FlexModels to provide necessary netlist compression with the accuracy and fast turnaround time needed to handle giga-scale designs

- Production-proven automated floorplan synthesis (Cadence First Encounter® technology) couples timing, power, area, and congestion-aware placement with fast global routing and in-place optimization, so you can quickly generate prototype floorplans
- A new automatic macro placement capability generates macro placement results that are convergent with implementation
- Built-in editing capabilities such as relative floorplan (specifying relationships for pre-routes, resizable objects, multiple relations, datapath stacking, integrated analysis tools) and resize floorplan help you quickly and accurately reach an optimal final floorplan
- A floorplan ranking system automatically generates multiple floorplan scenarios in parallel and analyzes them based on pre-defined QoR criteria; you can explore as much of the physical solution space as possible and make the most informed tradeoffs
- System designers can link into EDI System from Cadence Chip Planning System to bring physical predictability into their estimations

Silicon virtual prototyping and hierarchical support

Full-chip flat prototyping delivers complete physical, timing, clock, and power data, eliminating the guesswork associated with traditional block-based approaches. Hierarchical support helps physical designers assess how best to partition the logical hierarchy into physical modules. You can analyze the optimal pin assignments, budget time quickly, predict the clock distribution networks accurately, analyze the power grids, and generate complete timing and physical constraints for each of the physical modules.

Hierarchical implementation and closure

GigaFlex technology extends FlexILMs and FlexViews for concurrent top- and block-level optimization and final hierarchical closure. With FlexILMs, EDI System can optimize the top-level design concurrently with interface logic of block-level partitions, resulting in fewer iterations and a faster path to accurate budgeting and hierarchical convergence. In addition, FlexViews work at the post-route stage, providing late-stage hierarchical closure by allowing EDI System to optimize top-level paths together with inter-partition paths that are timing critical. This reduces the number of iterations taken to close top-level timing with block-level timing, resulting in a significantly shorter overall design turnaround time.

Multi-mode/multi-corner signoff ECO

MMMC signoff ECO provides a fully automated, physically aware, timing ECO capability applicable to the full-chip level. Using a highly efficient multi-CPU backplane coupled with a fast and accurate parasitic extraction engine, MMMC signoff-driven ECO automates static timing analysis, optimization, and retiming of all timing views in the design. It is based on timing-critical paths reported by the unified timing signoff engine, leveraging the same engine to perform timing ECOs in order to fix remaining violations. This high-capacity signoff ECO solution is optimized for execution on up to 100 timing views and has the performance to handle giga-scale designs at the full-chip level, greatly reducing the effort, the number of ECO iterations, and the closure time required for post-route design closure on timing ECOs.

Advanced Analysis Engine

At the design implementation and signoff stage, EDI System now leverages an Advanced Analysis Engine (AAE) that performs timing and SI delay calculation in a single step throughout the flow. AAE is built from the ground up, on a multi-CPU and multi-threaded infrastructure that enables near-linear scalability on eight CPUs. This significantly speeds up timing and SI analysis, IPO, clock mesh analysis, and all timing-related analysis throughout the flow, resulting in faster timing convergence for design closure.

Mixed-Signal Design

The amount of analog circuitry on SoCs is multiplying and, at the same time, the use of digital control logic inside analog blocks is growing. The result: blurred boundaries between "analog" and "digital." The Cadence Mixed-Signal Solution, utilizing OpenAccess as a single design database, enables analog and digital designers to retain their own preferred design environments while increasing implementation efficiency through easy and seamless data transfer between Virtuoso and Encounter platforms. Both analog and digital teams can easily see the complete design and any changes implemented by their peers, enabling efficient full-chip optimizations that were previously unobtainable.

This additional interoperability has proven extremely valuable when both analog and digital design teams need to carefully coordinate and agree on potential modifications—simply saving the database allows everyone to see the latest status in their own environment. ECOs can be managed more easily since they no longer require the generation of LEF/DEF/GDSII files to communicate the changes.

Comprehensive full-chip static timing analysis (STA) has always been challenging for mixed-signal designs, typically because custom/analog designers have to manually create Liberty (.lib) files for their completed mixed-signal blocks. EDI System has a unique ability to perform comprehensive STA by transcending the analog hierarchy and abstracting the digital logic and paths.

The Cadence Mixed-Signal Solution combines all of the strengths of EDI System—design closure, signoff analysis, advanced node design, low-power design—with the industry-standard Virtuoso Design Implementation platform for custom/analog design, enabling a total mixed-signal implementation solution that is second to none.

Advanced Technology Integration

20nm digital implementation and signoff methodology

20nm process technology signifies the next step in semiconductor process-node evolution. Due to the power, performance, and area benefits that 20nm provides at a process level, companies that adopt 20nm methodologies ultimately will be able to produce differentiated products that are faster, more integrated, smaller, and with more functionality.

However, adoption of 20nm process technology requires design teams to be well-equipped with a digital implementation and signoff methodology that can address the process requirements and timing complexity of 20nm, including double-patterning.

EDI System 11 introduces 20nm design implementation and signoff capabilities with correct-by-construction double-patterning support. These double-patterning capabilities span floorplanning, placement, optimization, routing, parasitic extraction, and signoff for timing, power, and physical verification of 20nm designs.

- Placement engine optimizes cell placement for double-patterning requirements, leading to better area efficiency
- NanoRoute® Advanced Digital Router with FlexColor technology routes in a correct-by-construction manner; metal is routed to be DRC and double-patterning–correct using a built-in physical verification engine during all stages of routing
- Cadence QRC Extraction produces multi-value SPEF files required for litho-biasing support and mask-misalignment modeling; Encounter Timing System utilizes min. and max. capacitance values on early and late launch and capture clock paths for Setup and Hold timing analysis; Encounter Power System utilizes multi-valued SPEF parasitic for power, IR drop, and AC/DC EM analyses
- Encounter Timing System considers intrinsic waveform effects during signoff timing analysis, including back-miller current effect that acts as an aggressor to affect timing delay
- Cadence Physical Verification System provides in-design signoff for DRC and double-patterning conflict checks

Advanced process variation support

In addition to providing foundry-supported signoff technologies for timing, SI, and power during implementation, EDI System employs advanced on-chip variation (AOCV), which uses logic level and physical location to select the optimal de-rating factor. AOCV eliminates the excessive guardbanding associated with traditional de-rating and improves timing closure, and is available for timing analysis and optimization in EDI System 11.

EDI System also supplements traditional single- and multi-corner–based methods with powerful and accurate statistical static timing analysis (SSTA) that accurately accounts for variability of process parameters in a single run. Using effective current source models (ECSMs), EDI System identifies cells and nets on both clock and data paths that are sensitive to variations, and then determines the probability of timing failures over the full scope of the process window. This reduces pessimism and limits guardbanding, which in turn reduces both area and power consumption while improving chip performance.

SSTA and statistical leakage analysis and optimization capabilities further reduce design cycles by eliminating the need for multiple analysis runs. Designers can tape out with the confidence of using a foundry-endorsed statistical solution to achieve and improve their timing and power goals in silicon.

Design for yield

EDI System optimizes yield issues all the way from RTL to GDSII. At any point in the design flow, you can perform yield analysis, analyze multiple strategies that affect and improve yield, and optimize the design immediately in the context of all other optimization objectives (including timing, SI, power, and area). Design-for-yield (DFY) features include:

- Context-driven placement, which takes layout electrical effects into account during implementation, resulting in better chip performance
- Wire spreading, wire widening, double-cut via insertion, and single via reduction and optimization
- Critical area analysis and optimization
- True lithography distortion prevention and optimization, and CMP-aware metal fill
- A rich set of random and systematic visual analysis and text-based reporting vehicles

EDI System’s robust native DFY capabilities allow you to quickly and accurately predict manufacturing variability and to make intelligent tradeoffs during prototyping and implementation for maximizing yield.

Design for manufacturing

Starting at the 45/40nm process node, design for manufacturing (DFM) is a mandatory step in the IC design flow. Traditional methods of addressing DFM variability issues at signoff are impractical; they cannot handle increasing design complexity and they have long turnaround times. Advanced node design requires starting with the end in mind; it requires in-design DFM to scale diverse design needs from blocks and IP to large SoCs.

Encounter in-design DFM focuses on maintaining designer intent and leveraging accurate abstraction of manufacturing issues to deliver fast silicon convergence for DFM variability hotspots. Production-proven, silicon-accurate signoff DFM technologies are integrated with EDI System to minimize the risk of yield-limiting DFM hotspots and reduce the electrical variability impact early in the digital implementation flow.

EDI System users can leverage Encounter DFM’s advanced analysis capability, in which silicon failures or variability hotspots are abstracted into patterns while maintaining the original design intent. This accurate abstraction reduces the turnaround time for DFM check analysis during digital implementation with EDI System by 100x, saving several days of DFM error iteration cycle time from the signoff stage.

3D stacked-die support

Today, vertical chip packaging schemes are being extended to the system level. A 3D stacked-die design environment enables companies to use a heterogeneous process while achieving even smaller silicon and package footprint sizes and higher performance for interconnect-intensive designs. EDI System fully supports the design, verification, and implementation of 3D stacked-die designs using:

- A consistent, unified environment that leverages 3D-IC intent (configuration file) to drive creation, implementation, and verification of 3D stacked-die designs across digital, full-custom, and packaging domains
- A 3D stacked-die chip/package/test abstraction and methodology that provides the speed and scalability to optimize heterogeneous processes/dies
- In-design 3D-IC signoff extraction, timing, power, and thermal analysis across multiple dies to ensure fewer iterations and faster convergence

Concurrent chip/package co-design with flip-chip support

Proven through multiple customer tapeouts, EDI System's flip-chip floorplanning and implementation technologies enable the concurrent design of chip and package by including package constraints and parasitic effects while designing the IC. With support for multiple I/O methodologies, concurrent optimization of area and peripheral I/Os with core instances, automatic RDL routing with 45-degree support, and accounting for RDL layers during signal/power routing, EDI System eliminates the traditional manual steps in I/O placement and optimization

Platforms

- lnx86: Linux (x86 and x86_64) 32/64-bit
- sol86: Solaris (x86_64) 64-bit
- sun4v: Solaris (ultraSparc) 64-bit
- ibmrs: AIX (power) 64-bit

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

cādence®

Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**

© 2012 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, Encounter, First Encounter, NanoRoute, and Virtuoso are registered trademarks of Cadence Design Systems, Inc. All others are properties of their respective holders.