

Design for Manufacturability and Testability

Why DFM & DFT?

Design for Manufacturability

- A design methodology intended to ease the manufacturing process of a given product
- DFM issues account for a major portion of defect, reliability, and cost in lead-free products
- DFM is key to faster time to market and higher quality
- DFM is one factor that controls yield, and therefore, final product cost
- Major DFM issues that designers should keep in mind for lead-free implementation are
 - selection of board finishes,
 - selection of laminate materials and via-hole considerations,
 - reliability concerns,
 - component selection, and
 - backward- and forward-compatibility scenarios.

Why DFM & DFT?

Design for Testability

- DFT adds certain testability features to a hardware product design.
- The purpose of manufacturing tests is to validate that the product hardware contains no defects that could, otherwise, adversely affect the product's correct functioning
- DFT often is associated with design modifications that provide improved access to internal circuit elements such that the local internal state can be controlled (controllability) and/or observed (observability) more easily
- In addition to finding and indicating the presence of defects (i.e., the test fails), tests may be able to log diagnostic information about the nature of the encountered test failures.
- DFT tests can be used to find the presence of defects and log diagnostic information about the nature of the encountered test failure
- This diagnostic information can be used to locate the source of the failure.

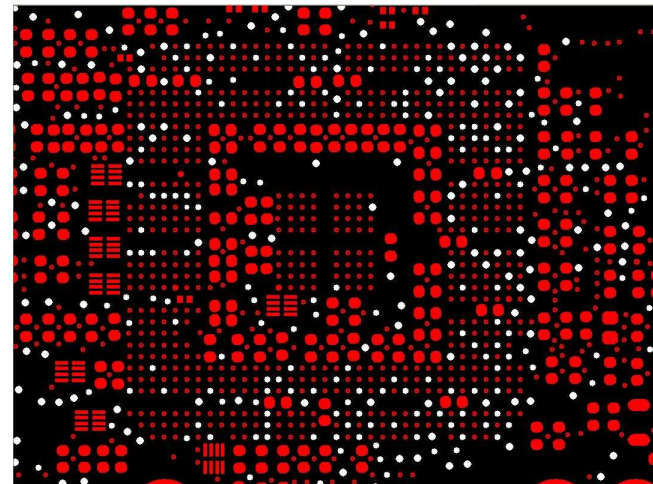
Common Design Problems

- To Provide 100% accessibility to a densely populated high speed board.
 - To provide accessibility to all the BGA pins and very small, fine pitch surface mount components
- To provide DFM to the board and achieve the best quality & cost effective manufacturing process
 - To understand manufacturing problems/issues of current/past products
 - To design for easy fabrication, processing, and assembly

Case Study – cPCI board

Specifications:

- Board size – 6U(233.5mm x160 mm)
- Total number of nets – 2350
- Total number of components – 2443
- Minimum trace width/spacing – 3.87 / 4 mils
- Minimum drill size – 10 mils
- No of layers – 14 layers
- Application – Telecom domain



Technology Involved

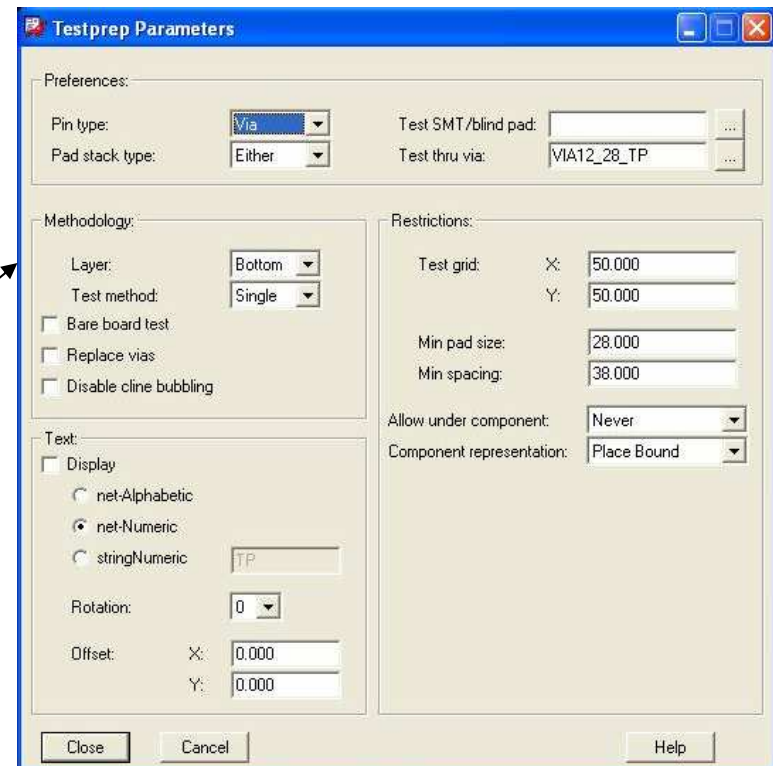
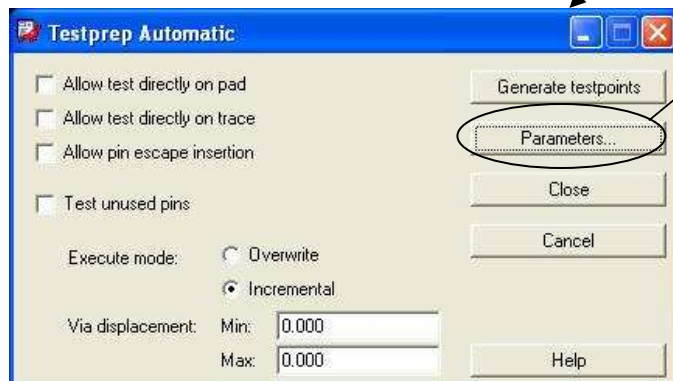
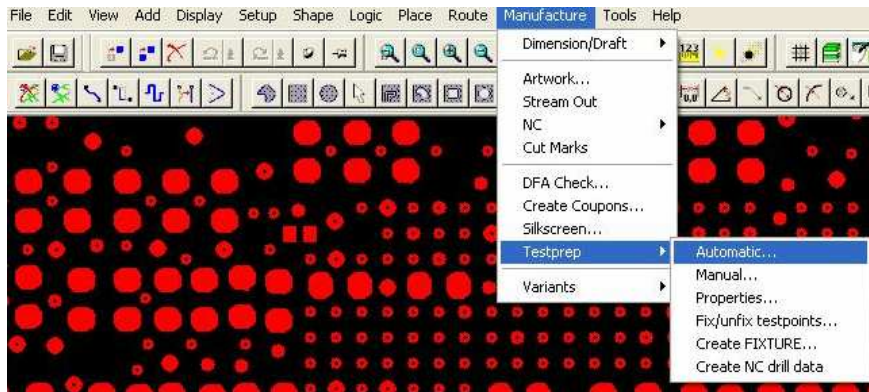
- Tools Used:
 - Allegro 15.2V
 - The required DFT constraints were clearly set in the parameters of the Test prep option
 - This assigned the test points automatically as per our requirements.
 - The reports were generated from Test prep Report generation option
 - This report gives the details of accessible and non-accessible nets in the board.

Technology Involved

- Tools Used:
 - Valor Enterprise 3000, 7.5V
 - Used different checklists to verify DFM and DFT. These checklists were filled as per the required constraints.
 - Assembly/Test Analysis programs - To deal with problems unique to assembly such as component spacing, fiducials, test points, outlines, etc.
 - Generated reports and Full automation for different categories in 5 major actions: Fiducial Analysis, Component Analysis, Padstack Analysis, Testpoint Analysis and Solder Paste Analysis.

Technology Involved

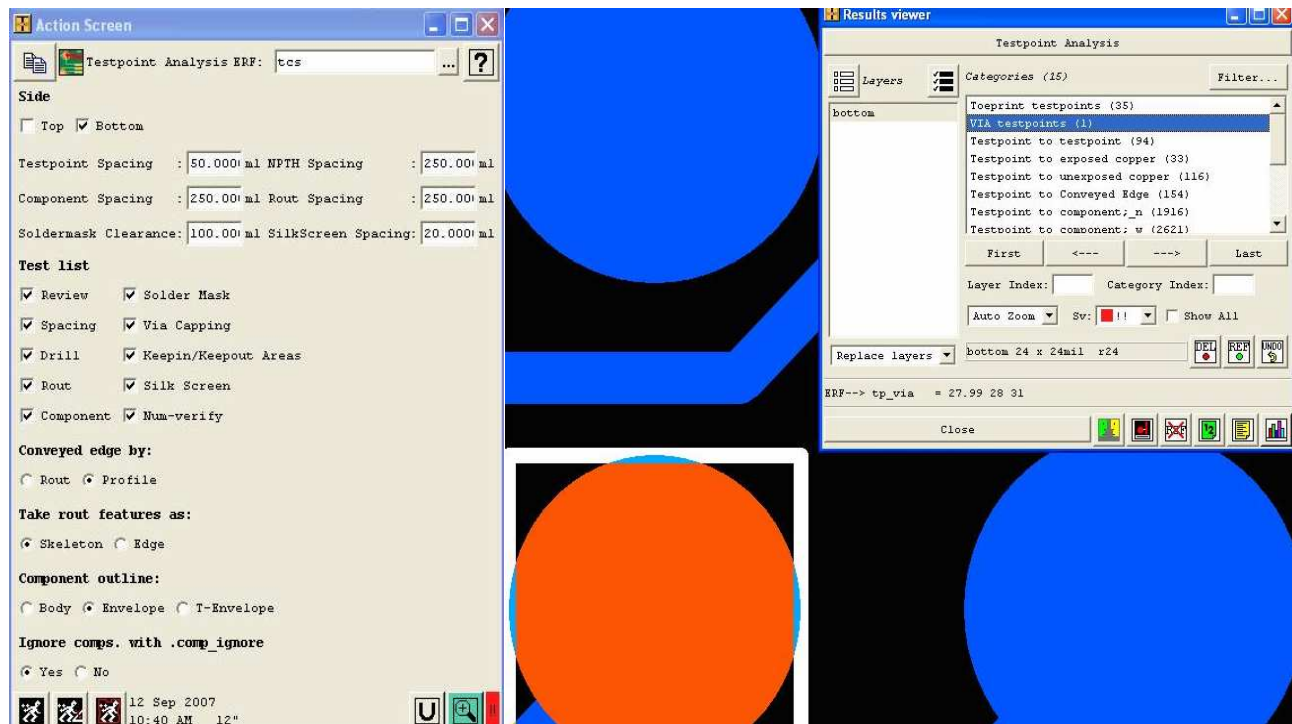
- Screenshots of the tool options used – Allegro



Technology Involved

- Screenshots of the tool options used – Valor

Used the Valor tool to check the percentage accessibility of the board and DFT constraints

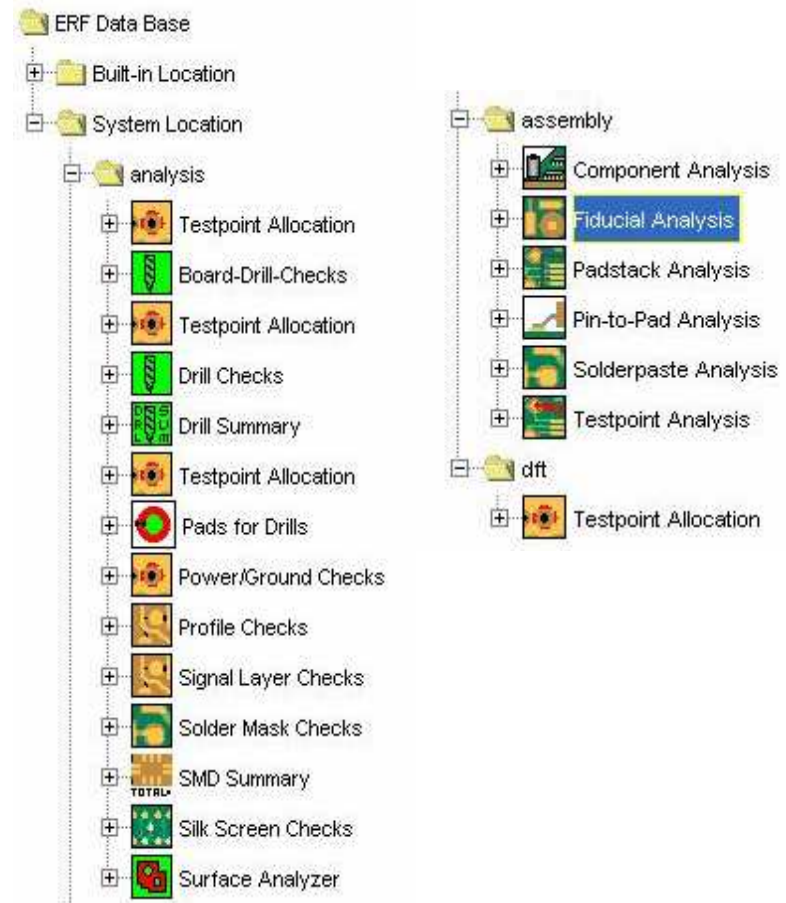


Technology Involved

- DFM analysis

Manufacturing constraints are set and verified using the Valor tool

- All the routing layer were checked for minimum trace to trace spacing
- Drill checks were performed for different drill size. It was cross checked with the drill table.
- Silk screen checks were performed to ensure no legend is falling on the component pads



DFM & DFT Constraints

- Vias were placed very close to each other due to high routing density. Because of this all the Vias couldn't be used as test points.
- Minimum center to center Test Point Spacing required was .050" (1.27mm).
- The fixtures to be used for the testing were of .039" (1.0mm).
- High Speed Signals that are 100 MHz and greater should not have a stub connection to the Test Point.
- All test Points were to be placed on the bottom side of the board as the top side probing is very expensive and proven to be un-reliable. Bottom side probing ensures that the tests are reliable and cost effective.
- To provide more than 3 mil spacing between the Land Patterns and Via or Land Pattern to Land Pattern
- To reduce the process cost, through-hole components were identified and replaced with the SMD components wherever possible.
- Fasteners had components placed perpendicularly to the fastener head. There were 8 of them.

DFM & DFT Constraints – Checklists & Reports

Checklist 1

- Component Selection
- Mechanical Considerations

Checklist 2

- ICT Considerations
- Boundary Scan Considerations
- FAT Considerations

Reports Generated - Valor

- Test point report for accessibility

```

Testprep_Report_temp.txt - Notepad
File Edit Format View Help
=====
|
|                                     Testprep Report
|
| Nets currently under test for TOP side ...
|
|-----|
| Net Name | QUANTITY | Number | Type | Pad Size | Location
|-----|
| Reference Designation |
|-----|
| Total number of testpoints on TOP side = 0
|
0|-----|
|
| Nets currently under test for BOTTOM side ...
|
|-----|
| Net Name | QUANTITY | Number | Type | Pad Size | Location
|-----|
| Reference Designation |
|-----|
| (Dummy-Net) | | 1 | via | 28.000 | 2433.000,941.500
| | | | | |
| | | | | |
| | | | | |
| | | | | |
|-----|
| V_0SENSE1 | | 1 | via | 28.000 | 1619.000,3836.000
|-----|
| V_NetA | | 1 | via | 28.000 | 171.000,3576.000
|-----|
| WDE_N | | 1 | via | 30.000 | 8020.000,2458.000
|-----|
| XVPIO | | 1 | via | 28.000 | 183.000,1493.000
|-----|
| Total number of testpoints on BOTTOM side = 2350

```

Benefits

- Best practices followed to achieve 100% DFT & DFM right the first time
- Streamlined the production
- Reduced DPMO introduced by PCB manufacturer capabilities and SMT process limitations.
- Reduction in the number of design iterations required
- Shorter time to market and a simplification of manufacturing processes with a consequent
 - Saved 2 – 3 weeks
- The purpose achieved:
 - Improved Quality product
 - Cost effective manufacturing process

Thank You