WHITE PAPER

NEXT-GENERATION SIGNOFF ANALYSIS TACKLES ELECTRICAL, PHYSICAL, AND MANUFACTURING CHALLENGES

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INTRODUCTION

The electronic design industry continues to push the limits of Moore's Law through smaller and smaller process nodes. As we reach 45nm, manufacturing and process control becomes increasingly difficult, making it imperative that manufacturability issues be addressed much earlier in the design cycle to avoid costly respins and chip failures.

Physical and electrical effects at this node challenge both design closure and time to market, and the requirements for design signoff are changing in order to address the inherent manufacturing and process variability. Naturally, this situation can seriously undermine the manufacturability of the design. In fact, a paradigm shift is evident in the all-important signoff analysis step of the digital design cycle.

At issue are the levels of validity and confidence that can be reached with today's IC design closure and signoff methodologies. Designs that pass traditional sign-off standards might still fail in 45nm silicon. In contrast, using excessive guard-bands or over-conservative margins to satisfy traditional static timing analysis (STA) signoff regimes can negate the benefits that smaller process geometries offer.

This paper looks at some of the electrical, physical, and manufacturing challenges to current signoff analysis methods, and shows new ways to improve predictability, productivity and performance at the 45nm process node. Using these new methodologies, designers can prevent silicon failures and better manage timing, leakage power, and signal integrity–both across a wafer and across the surface of a single chip.

TRADITIONAL SIGNOFF ANALYSIS–RUNNING OUT OF STEAM

Figure 1 illustrates how predictability in design schedules has diminished as the previously small, variable segment of the schedule has grown to dominate the overall schedule on complex projects at smaller process geometries.

If design complexity is normalized to 1X at 180nm, then design complexity at 65nm has significantly increased to 30-40X. Typically, design schedule variability is fairly contained at 180nm and is close to 10% over the planned design schedule. However, at 65nm the variable portion can be larger than the planned portion. And at 45nm, due to the advanced variation challenges, the schedule can potentially go completely out-of-control leading to major crisis situations.

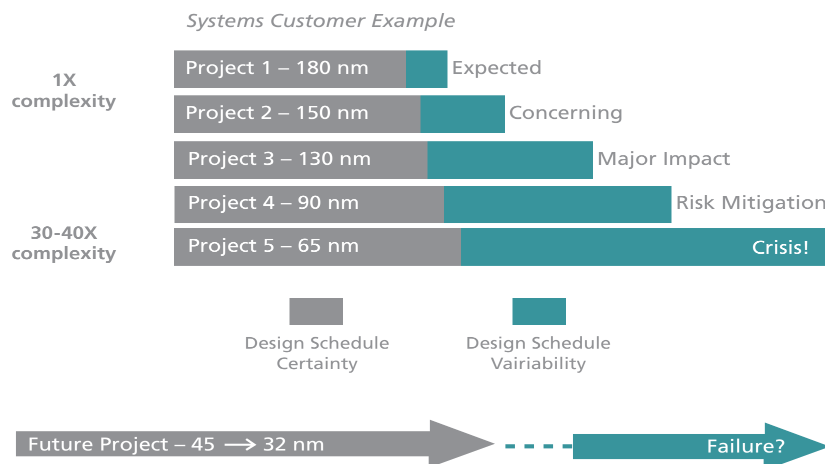

Figure 1. Nanometer Predictability Crisis

One strong reason for this lack of predictability and also a cause of diminishing productivity is the current disconnect between the analysis performed during implementation and the signoff verification required by the foundry. In addition to being utilized by completely different groups, the implementation and signoff tools employ different engines, which means the signoff analysis may detect problems that were not apparent during the implementation process. Fixing these problems can cause a ripple-on effect and generate new problems, which makes the process of achieving design closure extremely time consuming. Even worse is the fact that majority of today's implementation flows employ different engines for each of the tools in the flow. For example, the clock tree tool may use a different timing engine than the placement tool; in turn, the placement tool may use a different engine than the routing tool, and so on.

Another critical challenge for existing signoff solutions is the performance bottleneck brought on by the need to analyze an increasing number of electrical integrity and variability effects at 45nm. For example, the number of wires has increased significantly and so has the number of interactions between these wires. This leads to explosion in the number of signal integrity issues. Advanced techniques are needed to efficiently separate the handful of real problems from the plethora of false positives.

VARIABILITY IS THE ACHILLES' HEEL

The process of manufacturing an integrated circuit is inherently imperfect. Slight variations in the duration, temperature, and chemical concentrations at each step result in variations from one wafer to another, between die on the same wafer (inter-die), and between cells and interconnect on the same die (intra-die). These manufacturing variations result in physical changes in devices and interconnect leading to deviations in their electrical behavior. At 45nm process control is difficult, and even if the absolute amount of process variation remains the same as in previous generations, it accounts for a greater percentage change in overall performance at the smaller node.

Traditional static timing analysis (STA) cannot properly model the variability inherent in semiconductor processes. It compensates for this variability by requiring aggressive guard bands and by using multiple corners or scenarios to reflect different manufacturing conditions. But as the number of scenarios increases, the number of analysis runs can increase greatly, making design convergence exceedingly difficult while straining resources, increasing costs, and negatively impacting schedule. At the very minimum, current STA solutions need to have distributed processing capabilities to handle concurrent multi-corner analysis and thereby mitigate the compute burden. Unfortunately, the corner-based approach is also overly pessimistic since it can report timing scenarios that have an extremely small likelihood of occurring. For this reason, statistical static timing analysis (SSTA) is emerging as the signoff vehicle to carry the industry into the future.

SSTA–BRINGING SIX-SIGMA QUALITY TO CHIP DESIGN

SSTA makes it possible to break through the barriers of corner analysis and holistically model the many factors affecting process variation in a single analysis run. It enables designers to effectively model process and environmental variation, it obviates the need for multiple corners, and it removes much of the inherent pessimism. The statistical approach allows for reduced guard-banding, which results in decreased area, decreased power consumption, and improved chip performance.

With SSTA, designers can explore potential trade-offs and evaluate parametric yield for a desired performance target. The results are in the form of a probability density function (PDF), such as a normal Gaussian distribution, rather than a single slack value for each net like traditional STA. The

PDF curve indicates the probability of failure for a given timing slack. The sensitivities for device and interconnect, along with the distribution information for each process parameter, are used to generate PDFs for arrival time (data path), required time (clock path), and slack.

For example in *Figure 2*, consider a critical path arrival time of 2.3ns using the traditional worst-case corner methodology as shown by the right-most arrow marked "Worst Case". Instead, if the SSTA approach is employed as illustrated by the PDF curve, the designer can choose the 3-sigma

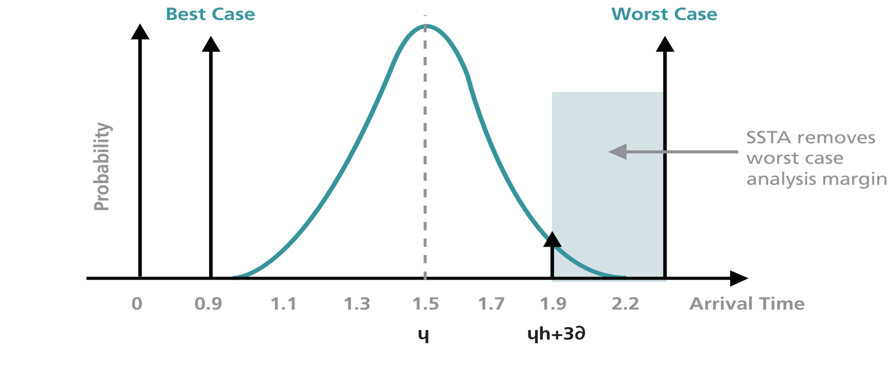

Figure 2. SSTA removes the worst case analysis margin

yield point which would provide a confidence level of 99.9%. This would result in the nominal arrival time of 1.9ns that effectively allows the designer to shave 400ps off of the cycle time–a path performance gain of 18.2%.

ACCOUNTING FOR SYSTEMATIC AND RANDOM VARIATIONS

Instead of applying a large safety margin to the entire design to account for local variations on all paths, the individual variations due to location and relative position on the die need to be modeled for each device and interconnect along a given path. Consider variations due to chemical mechanical processing (CMP), for example: they could cause a track in one area of the chip to be 15% thinner or thicker that an equivalent track located elsewhere on the chip. The two tracks would consequently have different resistances, which will affect their power dissipation and the speed of the signals propagating through them. *(see Figure 3)*

At 45nm, modeling the variation within the die is imperative for pessimism reduction on a path-by-path basis. This modeling should include systematic variation caused by CMP, lithography, mechanical stress, and etching effects. For lithography, for example, it should accurately model or

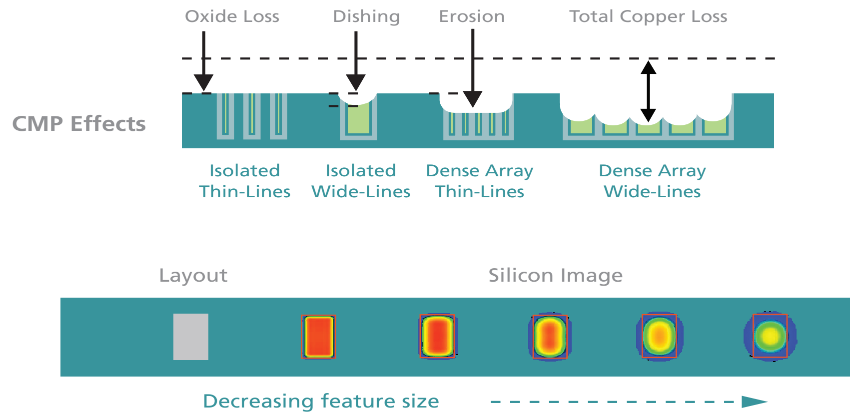

Figure 3. Systematic variation due to CMP and Lithography

simulate the way in which light will pass through the photo-masks and any lenses, how it will react with the chemicals on the surface of the silicon chip, and what the resulting structures will look like and how they will perform in silicon. The signoff solution then should be able to calculate the impact of these systematic effects on timing, signal integrity, power, area, and other performance parameters.

Devices also experience random or intra-gate variations, which can cause device mismatch. Spatial or mesh-based techniques should be used to model the amount of variation of interconnect and device parameters for different areas of the die. A spatial technique would involve defining how a particular parameter varies as a function of distance. A mesh-based technique can be employed by breaking the die up into a mesh and deriving a variation distribution for each parameter in each section of the mesh.

SIGNAL INTEGRITY – LOW POWER MAKES IT HARDER

In its most general sense, signal integrity (SI) means ensuring that signals faithfully propagate to their intended destinations within their allocated timeframes, even in the face of variation adversity. As SI capabilities have become incorporated into mainstream analysis and implementation tools, it is easy to be lulled into believing that SI is a solved problem. However, this is not the case. The new emphasis on low power design creates variations that must be addressed in SI analysis. In addition, significant improvements must be made to existing SI analysis techniques to reduce false errors which can lead to 45nm design closure nightmares.

Today's low-power designs typically make use of multiple supply voltages, and coupling from a higher voltage signal to a lower voltage signal is significantly more severe than coupling between signals of the same voltage. Low-power designs also use gates formed from transistors with different switching threshold (Vt) voltages. Higher Vt devices generally have a higher holding resistance, which makes them more vulnerable as victims of crosstalk. By comparison, lower Vt devices have faster transition times, which make them more aggressive as attackers. Another factor that comes into play with low-power designs is the need to turn on and turn off different sections of the chip to conserve power. This switching process generates transients in the power supply rails, which can affect operations in other parts of the chip.

Techniques such as noise propagation and path-based alignment have been applied in the past to reduce SI pessimism. However at 45nm, if the logical and timing correlation between aggressors and victims is ignored, it results in worst-case computations and excess SI pessimism. In *Figure 4* for instance, aggressor a5 affects victims v3 and v4, but worst case alignment for a5-v3 and a5-v4 may not be the same. Also, the aggressor a3 and aggressor a4 have opposite transitions while victim v2 and victim v3 have same transitions, so the SI delay push-out between a3-v2 must lead to speed-up in a4-v3. In addition, a3-v2 and a6-v4 can both be push-outs but the (a3, a4, a6) timing dependency may exclude simultaneous worst case alignments for a3-v2 and a6-v4.

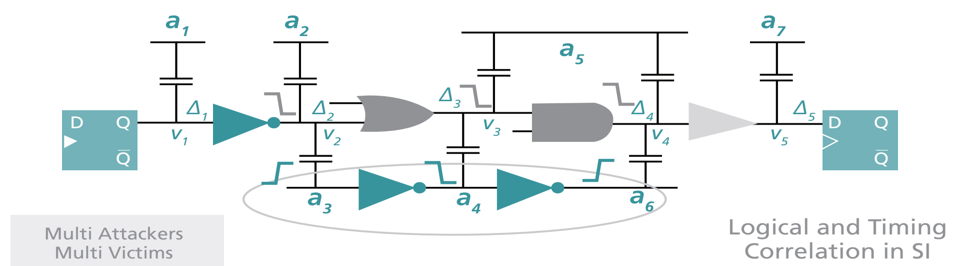

Figure 4. Noise Path Pessimism Removal (NPPR)

In a 45nm SI signoff solution it is important to employ Noise Path Pessimism Removal (NPPR) for these multiple-attacker, multiple-victim situations. NPPR accounts for logical and timing correlations between aggressors and victims while incorporating actual switching activity information to pinpoint the true SI problems, thereby allowing the designer to focus on the most likely failing paths.

THERMAL ANALYSIS–IT'S NOT ALL ARCTIC OR EQUATOR

A variety of factors at 45nm, such as increased power density and advanced low power techniques, have led to wider on-chip temperature gradients (variations). Depending on the amount of switching activity at any particular time, different areas of a chip may vary by 40ºC or more. Furthermore, the barrier layer on the top of the die acts as a "thermal blanket," with the result that there can be a thermal differential of as much as 45°C between the top-most layer of metallization and the inner surface of the silicon where the transistors reside.

The wider on-chip temperature variation needs to be taken into account in calculating critical chip metrics. Specifically, both chip timing and chip leakage power (and hence chip total power) are closely related to the temperature gradients on the chip. The temperature gradient on the chip, in turn, is affected by the power dissipation profile of the chip. In addition, the chip package has a big impact on the actual temperatures and the temperature gradients. *(see Figure 5)*

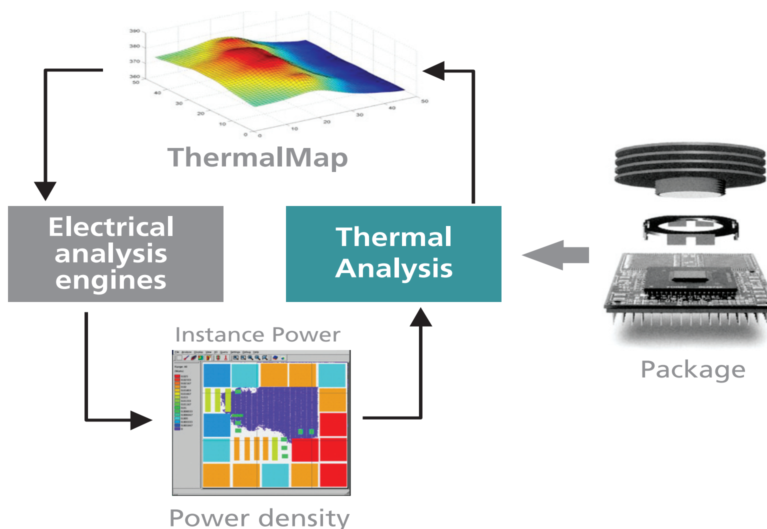

Figure 5: Thermal Analysis to tackle temperature variability

Attempting to guard-band against thermal effects means giving a lot away in terms of performance and power. In order to minimize this, the 45nm signoff solution should accurately model temperature gradients in the context of silicon, package, and board. This will allow designers to dramatically improve the accuracy of existing analysis and optimizations for power, voltage (IR) drop, electromigration, and timing.

ELECTROMIGRATION–THE MOVEMENT GETS WORSE

At 45nm, electromigration gets worse because current density (current per cross-sectional area) in a track is very high. The current flowing through a track causes the metal atoms in the track to migrate. This results in physical variations–areas of the track that are thicker or thinner than desired. In a worst-case scenario, the result will be a catastrophic failure caused by a short or an open circuit. However, even before this happens, the increased resistance associated with tracks that become thinner will result in a corresponding voltage drop, which will modify the timing, power, and noise characteristics of any affected gates.

In the past, electromigration has been of particular concern in the case of power and ground wires, because (a) they carry larger currents than do the signal paths and (b) their currents are always flowing in the same direction. However, at 45nm, electromigration effects become significant on signal wires and even in the logic cells themselves. The 45nm signoff solution should have electromigration analysis tightly coupled with the rest of signoff analysis.

SUMMARY

Designing at the 45nm node combines huge risks with the potential for huge rewards. In order to take full advantage of 45nm process capabilities, it is important to understand and quantify process and manufacturing variations to improve accuracy, reduce pessimism, and support informed decisions about yield and performance tradeoffs. To this end, the chip design industry must be prepared for a paradigm shift towards a signoff analysis that enables "Signoff for Manufacturability."

This new signoff solution will account for systematic and random variations, CMP, etch, lithography, thermal, and electromigration impact to evaluate timing, leakage, signal integrity effects. The more holistic SSTA approach will allow designers to mitigate the effects of process variation, prevent silicon failures, and meet the demands of cutting-edge electronic design for the foreseeable future. It will usher in the much-anticipated "electrical DFM" that provides multi-objective placement, physical synthesis, and routing optimization while comprehending the full spectrum of physical and electrical implications of manufacturing.

At 45nm, it is also imperative to use a single signoff engine that provides a uniform source and consistent view of timing, signal integrity, and power all the way through physical implementation to final signoff verification. The fact that the same timing engine is used for both implementation and signoff verification allows design engineers to perform "signoff in the loop"—significantly improving predictability, productivity and performance. The end result is simple: design teams that do not embrace this technology have a high risk of building chips that either don't meet their desired performance goals or don't work at all. By comparison, designers and verification engineers that use this next-generation "Signoff for Manufacturability" solution will be able to successfully design and build chips at 45nm and reap huge rewards.

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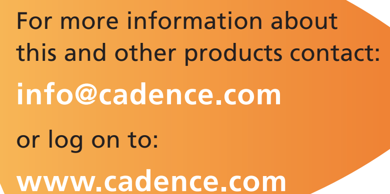

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