RF IC FLOW
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1 OVERVIEW

This document describes the radio frequency (RF) integrated circuit (IC) reference flow of the Cadence® Virtuoso® custom design platform. The Virtuoso custom design platform targets full-custom designs across the diverse domains of analog, custom digital, RF, and memory/array design. The platform also enables the integration of IP from these various domains, including importing digital standard-cell blocks with an integration strategy and methodology.

The Virtuoso platform is based on an overarching methodology that applies to each of the included design domains and all integrated blocks, and is designed to serve as a “blueprint” by which any platform targeting custom design can be measured.

The RF IC reference flow is based on the Advanced Custom Design (ACD) Methodology and is one flow element of the Virtuoso platform. The ACD Methodology document is available at cadence.com.

2 THE RF IC CHALLENGE

RF IC designers face several significant challenges. Large RF ICs, such as wireless transceivers, for example, comprise a full range of on-chip functionality that in particular stress functional verification solutions. In addition, high-speed requirements make RF circuits extremely sensitive to the effects of parasitics, including parasitic inductance, passive component modeling, as well as signal integrity issues. Thus, the essence of the RF IC flow is the ability to manage, replicate, and control post-layout simulations and effects and to effectively use this information in a timely fashion at appropriate points through the design process.

RF IC design also requires specialized and unique analysis techniques specific to RF design. These vary between frequency domain and time domain analysis methods, chosen on the basis of circuit type, designer comfort level, circuit size, and/or designer preference. Ultimately, this requires a seamless environment that facilitates choice in simulation method.

Integration trends have also affected the RF IC world, which used to be viewed as a separate, almost standalone entity. Today, many RF ICs contain at least the analog-to-digital converter (ADC), digital-to-analog converter (DAC), and phase-lock loop (PLL) functions, as well as a digital synthesizer, which is created through the digital environment and integrated on-chip. In some cases, RF content is being added to large systems-on-chip (SoCs) as design groups attempt a single-chip solution. Other design teams are integrating RF content by using system-in-package (SiP) techniques, which leads to similar verification issues as RF IC and SoC methodologies.

These advanced issues demand an RF IC solution that must:

- Optimize simulation time
- Facilitate verification
- Enable detailed analysis at the block and chip levels
- Manage and facilitate simulation with full parasitics
- Enable analysis (noise, IR, EM) early and often in the flow
- Include layout automation that can be used at appropriate points in the design
- Enable several levels of passive modeling throughout the design process

All of the above requirements must be met through a single environment that not only facilitates the job of the RF IC designer, but also integrates with the other domains such as analog/mixed-signal (AMS) and digital design. This environment must include both front-end and back-end perspectives at multiple abstraction levels, so that design collateral can be passed back and forth, facilitating verification/implementation from either point of view, independent of physical integration strategies.
THE ADVANCED CUSTOM DESIGN METHODOLOGY

The first place to start describing an RF IC flow is from a more global methodology perspective and context. The ACD Methodology is shown in Figure 1. This describes a process geared towards mixed-signal design, which takes design tasks and parallelizes them, allowing for a top-level perspective, for parasitic and analysis functions performed early and often, and which ultimately enables the design to progress with as much information as is available at any given point in time. Predictability is the driving force behind the ACD Methodology. The need for predictability is driven by two primary concerns: schedule, which must be met from the beginning of the design process, and which necessitates a fast path to tapeout; and performance requirements, which must be met to achieve first-pass success, and which require a silicon-accurate methodology.

![Figure 1: Methodology diagram](image)

SCHEDULE REQUIREMENTS: TOP DOWN

To meet schedule requirements, RF designers need a fast design process that supports thorough simulation and physical design. The top-down design process, when applied to both simulation and physical design, is the approach that facilitates a fast design process. The design process is comprised of many tasks, and many of today's chips contain multiple blocks from multiple design domains. Thus, it is imperative to design-in as many of these blocks and perform as many tasks as possible in parallel, leveraging as much of the top-level IP as possible throughout the process. This leads to the concept of design evolution, where all a design's IP is leveraged as it matures through the design process.

Using this concept, multiple abstraction levels — from high-level design through detailed transistor-level design — are combined to support a mixed-level approach that targets detailed design to only the point(s) needed for a given test. This also enables designers to leverage top-level information for block design, and to subsequently re-verify the blocks in the top-level context.

PERFORMANCE REQUIREMENTS: BOTTOM UP

To achieve the required design performance, RF designers need a design process that is silicon accurate. Silicon accuracy relies on base design data, such as device models, that support accurate simulation, and technology files that support physical verification and analysis. Test chips, which are often comprised of critical structures that are known from past designs to be highly sensitive, are also used in this process to verify the feasibility of a process and the accuracy of its corresponding process design kit (PDK). Often, a design group will need to add components to the PDK to support a particular design style. Device models may need to be expanded to combine or add corners, or to facilitate statistical modeling or other approaches the design team requires.
This silicon-accurate data is driven through the design process through detailed transistor-level analysis, including layout extraction. The calibration of these lower-level silicon-accurate results to higher levels of abstraction ensures that designs will meet performance requirements. This comprises the bottom-up portion of the ACD Methodology.

MEETING IN THE MIDDLE

In practice, the top-down and bottom-up processes work in parallel, producing a “meet-in-the-middle” approach. This meet-in-the-middle approach balances the need for a fast design processes with silicon accuracy, which ultimately produces a predictable schedule and leads to first-pass silicon success.

The ACD Methodology can be applied to a complex integration or to a particular domain area. The methodology for each domain applies the meet-in-the-middle approach, combining top-down speed with bottom-up silicon accuracy.

4 THE VIRTUOSO RF IC FLOW

The RF IC flow is depicted in Figure 2:

![RF IC flow diagram](image-url)

**Figure 2: RF IC flow**

The top-down process starts with HDL modeling for the entire RF IC. This includes all RF blocks, along with any analog content and/or digital blocks. The first step is to model behaviorally the full chip within a top-level testbench, which would verify some system tests such as error-vector magnitude (EVM) or bit-error rate (BER) tests. This step initially verifies the partitioning, block functionality, and ideal performance characteristics of the IC. This behavioral setup then serves as the basis to facilitate mixed-level simulations, where blocks can be inserted at the transistor level and verified in a top-level context. This full-chip setup can serve as the regression template to enable continuous verification as blocks mature, creating a continuous evolution approach through the entire design process. This is very important, because any problems can be detected at the earliest stage possible, when time still remains to fix the problem, and because blocks can be designed in parallel according to individual schedules.
Next in the flow, a preliminary circuit is designed, enabling early circuit exploration and a first-cut look at how the design meets performance specifications. This early exploration leads to a top-level floorplan, which for RF ICs is very sensitive to signal integrity concerns, and block-level interconnect design and parasitics. At this stage, it is possible to synthesize passive components such as spiral inductors to specification, and to do an initial placement of these on the chip. This enables two key activities: the creation of early models for spiral inductors that can be used in simulation before the block-level layouts are complete, and the initial analysis of mutual inductance between the spirals. Component models of each inductor can be generated within this context for use in these simulations.

Next, simulation is performed using the designer-preferred method, using either the frequency or time domain. This choice depends on the circuit, type of simulation, amount of design data to be simulated, and is a judgment call by the designer. A single process design kit and associated environment enables a smooth determination and selection of the simulation algorithm desired. Results are presented through a display appropriate for the selected simulation type. As circuits are completed at block level, they are verified within the top-level context with behavioral stimulus and descriptions for the surrounding chip. Simulation setups are created and kept in a specification-driven environment, which enables effective management of numerous simulations and views of each block. The full simulation environment will comprise several views of the same circuit. These are likely to include a behavioral view, a pre-layout transistor-level view, several views of parasitic information (one view may have resistance and capacitance (RC) only, one view resistance, inductance, and capacitance (RLC), one view RLC plus substrate, etc.), and perhaps a backannotated behavioral view. The specification-driven environment provides the means to manage all these simulations, pick the appropriate views of each block or sub-block, and manage the runtime vs. accuracy tradeoffs for the simulations that are being performed. This provides an effective mechanism to setup the continuous regressions that support the ACD Methodology.

As blocks mature, more transistor-level information may be required to test RF/analog and RF/digital interfaces. These tests will require the use of a mixed-signal simulator capable of handling analog, digital, and RF descriptions and a mix of behavioral-level and transistor-level abstractions. Runtime vs. accuracy tradeoffs can be made through simulation options; the designer can send the transistors to a FastSPICE simulator, or keep the transistors in a full SPICE mode. This configuration is highly dependent on the circuit and sensitivity of the interfaces. The ability to manage these configurations effectively is important as they must be repeatable.

Layout automation (automated routing, connectivity-driven layout, design-rule–driven layout, and placement) can be used judiciously. The advantages to using layout automation are that it is tied to the schematic and design-rule-checking (DRC) rules and that it enables productivity gains. Analog-capable routers can help with differential pairs, shielding wires, and enable manual constraints per line. This enables a physical design process that can become just as repeatable as the front-end process. The time and overhead expended to setup the initial tools is made up as iterations are made through the design process. Engineering change orders (ECOs) are performed more effectively if a repeatable layout process is in place. The repeatability of an automated layout process is weighed against the requirements of highly sensitive circuitry, which demands a manual approach.

As layouts are completed, electromagnetic simulation (EM) can be used to provide highly accurate models for passive components. For example, several spiral inductors may be selected as highly critical and a target for EM simulation. These EM simulation models can be swapped in to replace the models that were created early in the design process, and can be mixed and matched with the existing models. This gives the designer full control over the spiral modeling process, and again enables the ability to tradeoff runtime vs. accuracy.

Net-based parasitic extraction becomes a key element of the process as layouts emerge. RF design is highly sensitive to parasitic effects. The ability to manage different levels of parasitic information is paramount, as the designer can describe the amount of parasitic information to include for each area, line, or block. Less sensitive interconnects may require RC only, where more sensitive lines may require RLC. Lines with spirals attached can be extracted fully with RLC plus the associated inductor component, and substrate effects can be added for those lines that are the most sensitive. Again, those lines that contain a “full” extraction can be mixed and matched with the component models for passive components that were created earlier.
Managing drawn inductors through the parasitic extraction process is an important aspect of a complete design flow and warrants special consideration. In fact, one can consider inductor creation to follow the meet-in-the-middle methodology. Early in the design process, these inductors are drawn (or synthesized) using a top-down model. As the design progresses, and as layouts mature, the bottom-up process enables more refinement. At this bottom-up stage, full parasitic effects—including substrate—are included for the inductor as well as the surrounding circuitry using the same parasitic methodology as the rest of the circuit. This enables more accurate representation of these critical components.

Circuit designers need the ability to choose the method most appropriate in the up front process: a quick, quasi-static equation-based solver; or a slower, more accurate 2.5-3D EM full-wave numerical solver. Both can compliment the design process from inductor synthesis to final check. There should be reasonable agreement between the methods for well-characterized semiconductor processes in the lower-frequency regimes. The full-wave EM solutions are better for complex shapes and higher-frequency harmonics. But all circuits do not have these needs. The full parasitic check at the end serves as the signoff, net-based extraction, and models from these various solvers can coexist with the extracted data. Discrepancies may arise, and understanding any discrepancies is an important step as a variety of situations depending on process information and setups could impact the models and simulation results. In this case, there is great value in having multiple simulation runs from different stages and using various techniques to ensure accuracy.

Finally, as blocks are completed, the initial behavioral models can be backannotated for key circuit performance parameters, which can provide a more accurate HDL simulation. While this backannotation will not account for every effect, it can add more realistic performance information at a very small runtime cost, enabling faster high-level verification, and perhaps reducing the amount of full transistor-level verification required.

5 SUMMARY

The RF IC flow is a key element within the Virtuoso platform, enabling full-scale, front-to-back RF IC design. Based on the ACD Methodology, the RF IC flow combines the meet-in-the-middle approach with the extreme sensitivity required for the design of high-performance RF circuits. The versatility in the RF IC flow interaction with other solutions such as the AMS and physical integration flows enables designers to apply the right solution to the right design task.