Introduction

Cadence led the industry with the formation of the Power Forward Initiative and the introduction of a complete RTL-to-GDSII low-power solution enabled by the Silicon Integration Initiative’s (Si2’s) Common Power Format (CPF) more than six years ago. At that time, the industry was not quite sure whether the power intent side-file approach was the right methodology to address the challenges of advanced low-power design. At present, the Cadence® Low-Power Solution has achieved wide adoption and has been proven by hundreds of design tapeouts around the world. Many prestigious companies—such as ARM, Fujitsu, Faraday, GUC, Hisilicon, SandLinks, STARC, and TSMC—along with numerous third-party tool suppliers—including Apache, Atrenta, Calypto, and SpringSoft—have adopted the power intent side-file approach and endorse the Cadence Low-Power Solution publicly. For more success stories about customers using the Cadence CPF-enabled solution, visit the official Power Forward Initiative website and download “A Practical Guide for Low-Power Design.”

Fundamental Differences Between UPF and CPF

An alternative power format in the industry is IEEE 1801-2009, which includes the Accellera Unified Power Format (UPF) 1.0. Although UPF 1.0 shares similarities with CPF, it has some fundamental differences in how the power intent is defined. In CPF, power intent is primarily described by an abstract data object called a power domain starting at the register transfer level (RTL). As the design flow evolves from RTL design to physical design, each power domain will eventually be refined into a primary set of power supplies to uniquely define this power domain. UPF 1.0, however, lacks such abstraction capability, so an RTL designer using UPF 1.0 has to describe the exact physical power network at RTL. The main difficulty of this approach is that RTL designers do not have the complete physical power network information.

There are other major differences between UPF 1.0 and CPF, such as how the isolation and level shifter logic between power domains is defined. IEEE 1801-2009 introduces the concept of the supply set, which has many similar
properties to the power domain in CPF, and many other constructs to close the methodology differences between UPF 1.0 and CPF (such as the way to specify isolation and level shifter logic using the driving/receiving power domain of a signal).

An example of a simple design with two power domains. The top design has one external supply VDD and one of the internal blocks uses the switched version of the top supply, controlled by the signal pon at the top level.

Figure 1: A simple design with power gating

To describe the above design using UPF 1.0, the power intent file would be as follows:

```plaintext
create_power_domain PD_blue –include_scope
create_power_domain PD_green –elements { I1 }
create_supply_net VDD –domain PD_blue
create_supply_net VSS –domain PD_blue
create_supply_net VDD_SW –domain PD_blue
create_supply_port VDD
create_supply_port VSS
connect_supply_net VDD -port VDD
connect_supply_net VSS -port VSS
create_supply_net VDD_SW –domain PD_green –reuse
create_supply_net VSS –domain PD_green -reuse
set_domain_supply_net PD_blue –primary_power_net VDD –primary_ground_net VSS
set_domain_supply_net PD_green –primary_power_net VDD_SW –primary_ground_net VSS
create_power_switch PSW –domain PD_blue 
  –output_supply_port {vout VDD_SW} –input_supply_port {vin VDD} 
  –control_port { control pon } –on_state {on vin control} –off_state { off !control}
```

Figure 2: Power intent in UPF 1.0

As indicated by Figure 2 above, designers using UPF 1.0 have to lay out almost the complete physical power structure at RTL, which is not only a difficult task but also a completely unnecessary one. Using the power domain concept in CPF or the supply set construct in IEEE 1801, the power intent of the example design can be described easily at RTL, as shown below:

**Power Intent in 1801**

```plaintext
create_power_domain PD_blue –include_scope
create_power_domain PD_green –elements { I1 }
add_power_state PD_green –state off
  {-supply_expr {PD_green.primary.power == OFF}
   -logic_expr { !pon }}
create_power_domain PD_blue –default
create_power_domain PD_green –instances { I1 }
  -shutoff_condition { !pon } 
  -base_domains PD_blue
```

*Note: in this example the implicit supply set of power domain PD_green is used, referred to as PD_green.primary.

Figure 3: Power intent in 1801 and CPF

It is clear that the methodology to describe power intent at RTL by using either CPF or the new constructs in IEEE 1801 is a much better approach than that of UPF 1.0. Unfortunately, the IEEE 1801 standard has included all the constructs from UPF 1.0. As a result, within the same standard there are two radically different methodologies to describe the same power intent. Such a mix of methodologies in the same standard not only creates confusion for users but also adds unnecessary difficulties for tool vendors to support the standard. It is no surprise that two years
after the release of IEEE 1801-2009, there is still a lack of tool support for the new 1801 methodology for power intent creation. Many EDA tool vendors who already support UPF 1.0 have chosen merely to continue with the Accellera UPF 1.0 approach for their support of the IEEE 1801 format.

This explains why designers who want to use IEEE 1801-2009 are pressuring vendors to support the true essence of the 1801-2009 specification, not just the UPF 1.0 method that was included in the initial 1801-2009 specification for Accellera compatibility. There are strong signs both within the EDA industry and the user community that the momentum is finally shifting to facilitate this change.

The following picture demonstrates the current status of all power standards:

![Current status of all power standards](image)

**Figure 4: Current status of all power formats**

### Power Format Convergence Requires Methodology Convergence

To achieve full interoperability among different vendors supporting different power formats, the methodology differences between CPF and IEEE 1801 must be addressed. Cadence supports the effort to develop a converged power methodology with the IEEE 1801 Working Group. There are two major objectives to be achieved through this effort. First, IEEE 1801 needs to define a process to censure the incompatible methodology as enabled by some UPF 1.0 constructs (such as power supply net–driven power intent specification). Second, the Si2 needs to contribute the Open Low-Power Methodology, or OpenLPM, which consists of a set of unique CPF features that are currently not available in IEEE 1801. One such feature is the formal hierarchical design approach, including macro modeling for hardened intellectual property (IP).

To facilitate this methodology convergence effort, Cadence joined the IEEE 1801 Working Group as a voting corporate member. The effort has already gained wide industry support, including from heavyweights like TI, Qualcomm, LSI, and STMicroelectronics. It will benefit all EDA suppliers, as it eliminates redundant investment in multiple and conflicting methodologies and formats.

### Cadence Low-Power Solution

The Cadence Low-Power Solution currently enables mixed tool flow interoperability through support for UPF using an import feature in the Encounter® Conformal® Low Power product. Conformal Low Power can import a UPF file along with the corresponding design and library, and export a semantically equivalent CPF file. The CPF file can then be used by other Cadence tools to continue the design flow. This approach has been successfully used by several customers on real production designs.

Until the converged methodology becomes a reality, Cadence will continue to provide format interoperability using Conformal Low Power import support for IEEE 1801-2009. We will also continue to invest in CPF and the CPF-enabled Cadence Low-Power Solution. As such, customers who have already adopted CPF are assured of a more robust and mature Cadence solution going forward. For those who are not currently using CPF but who would like to benefit from its differentiated features, the production-proven Cadence Low-Power Solution will provide the needed support for immediate design use. And for all users, the IEEE Working Group’s methodology convergence efforts ensure that their current and ongoing investment in CPF will be leveraged even after the converged methodology is available.

The CPF-enabled Cadence Low-Power Solution has been leading the industry with its comprehensive and mature technology (see Figure 5). The classical technologies included in the solution are Incisive® Enterprise Simulator (for low-power functional verification), Virtuoso® AMS Designer (for power domain–aware mixed-signal simulation), Encounter® RTL Compiler (for power-aware logic synthesis and design-for-test synthesis), Encounter Conformal Low Power (for power-aware formal verification), Encounter Test (for power-aware automatic test pattern generation), Encounter Digital Implementation System (for power-aware physical implementation), Encounter Power System (for power integrity signoff analysis), and Encounter Timing System (for timing signoff).
Most recently, Cadence added Virtuoso and Palladium® technologies into the CPF-enabled solution suite. Automatic CPF import/export in the Virtuoso environment enables static verification of the power structures of a schematic using Conformal Low Power. CPF-enabled emulation and hardware acceleration in the Palladium system is the industry’s only solution that addresses system-level verification of power management using real system software or applications.

**Summary**

Cadence will continue to invest in low-power design technologies that deliver unique value to customers. We are also committed to supporting customers with mixed power format flows. The UPF import capability in Conformal Low Power can be used to address the immediate needs of customers using UPF who also want to benefit from part of the Cadence Low-Power Solution. Over the long term, Cadence is dedicated to the methodology convergence effort at IEEE and Si2, and we intend to fully support the converged methodology standard once it becomes available.

**Resources**


