



IMPLEMENTING THE FASTEST PATH
FROM CONCEPT TO CONSUMER FOR
ADVANCED-NODE ICS

OVERVIEW

In a market driven by a growing consumer appetite for more sophisticated products, semiconductor companies are moving quickly toward advanced node technologies at 45nm and below. Bringing significant advances in silicon real estate and performance, these technologies promise new levels of integration of complex applications in system-on-chips (SoCs). As more designs move to advanced technologies, however, semiconductor companies face dramatically greater design challenges and a growing risk of failing to ensure rapid time to volume.

By combining new methods for design, development, implementation, analysis, signoff, and manufacturing, Cadence offers an evolutionary approach to design that delivers the revolutionary results needed for high-volume production of next-generation designs. By helping semiconductor companies designing at advanced nodes prevent manufacturing problems early—during the design stage itself—the Cadence® Advanced Node Design solution delivers the comprehensive approach needed to ensure the fastest path from product concept to consumer delivery.

In the move to the next generation of manufacturing technologies, engineering specialists must contend with a spiraling list of technical concerns. Fabricated in more complex manufacturing processes, sub-wavelength devices present greater challenges to designers needing to predict performance in an environment of increased process variation, defects, and manufacturing effects. Larger designs mean significantly bigger datasets to account not only for more transistors but also for increased data associated with the growing array of electrical and physical effects that will significantly impact 45nm design performance.

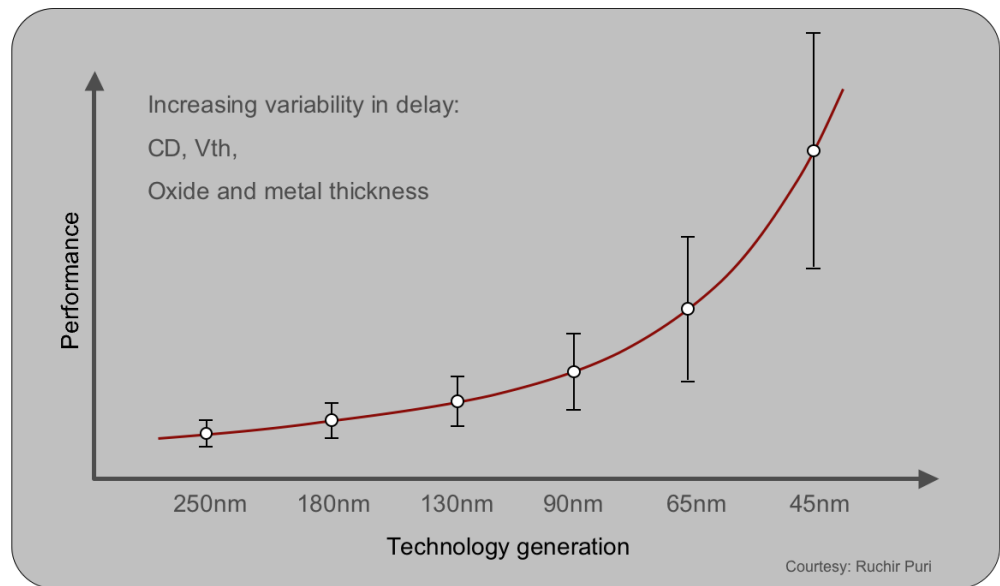


Figure 1. Delay variability increases with each process generation as process variation widens.

As shown in *Figure 1*, manufacturing effects that could be safely ignored with older generation technologies exert a greater impact on design performance with newer technologies. For designs below 90nm, conventional delay calculations are no longer accurate. Designers require more powerful analysis methods and more sophisticated models that account for manufacturing variation over a broader process, voltage, and temperature (PVT) envelope. Then, during physical design and fabrication, engineers require flexible development methodologies capable of maintaining design objectives throughout a more complex manufacturing process.

The requirements of advanced node design have driven a fundamental change in physical design signoff. With 45nm designs, design-rule check (DRC) does not provide designers with sufficient information to meet yield requirements. Semiconductor companies can no longer expect to meet performance and yield objectives with a late manufacturability signoff during the final DRC check. Unlike previous signoff phases (such as timing signoff and power signoff), manufacturability signoff must occur throughout development all the way from concept to customer, using preventative measures and optimization to avoid expensive silicon debug and design respins, as shown in *Figure 2*.

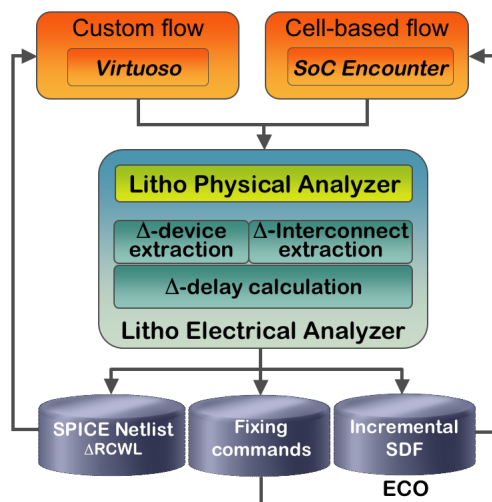


Figure 2. To prevent expensive problems late in development and to optimize performance and yield, semiconductor companies need to draw on sophisticated analysis capabilities and apply manufacturability signoff from product concept to consumer device.

COPING WITH INCREASING VARIABILITY

In previous technology generations, designers could build in margin to compensate for simplified design rules and manufacturing variations arising primarily from via failures and random particle defects. With advanced node manufacturing, designers face a broadening range of systematic and random variation, introducing effects that dramatically impact silicon performance and cannot be countered effectively with increased margin. Without capabilities to model these effects and take preventative measures early in design, designers face silicon failures with few corrective alternatives.

Even familiar effects due to lithography and chemical-mechanical planarization (CMP) exert a greater impact on circuit electrical characteristics with advanced node technologies. For older technologies, the microscopic imperfections in planarization following CMP could be safely ignored or addressed with additional margin. At the miniscule dimensions of modern processes, however, CMP imperfections represent significant variations in the true thickness and contour of each layer. These variations can cause both timing failures and catastrophic yield loss from copper pooling, for example.

Similarly, designers have grown increasingly familiar with the growing impact of resolution enhancement technologies (RET) during post-processing of GDSII design files. RET methods such as optical proximity correction (OPC) and phase shift mask (PSM) are used to correct distortions arising from the use of 192nm wavelength light to draw sub-wavelength features during the lithography process. As semiconductor manufacturers moved to more advanced nodes below 192nm, designers found themselves forced to anticipate these lithographic effects on silicon performance.

At 45nm, lithography effects have become more dramatic and varied. For advanced-node ICs, designers cannot expect accurate analysis results using previous generation mechanisms for extraction of critical parasitic parameters based on drawn shapes in layouts. The systematic variation between geometric and actual shapes for both transistors and interconnects in these advanced node designs translates into significant differences in parasitics—differences accentuated by the electrical characteristics of high-performance 45nm devices.

Beyond these more familiar effects, advanced node technology introduces an array of new effects that complicate reliable prediction of silicon performance. As sub-wavelength lithography continues to shrink gate length, semiconductor materials specialists have adopted new techniques to restore performance to these smaller devices. Among these techniques, the introduction of stress and strain in the transistor gate area improves individual transistor performance, but also introduces changes in the carrier mobility of neighboring devices. As a result, engineers can see large variations in performance for devices in different neighborhoods experiencing different stresses.

At 45nm geometries, other effects also introduce additional placement-related variations. For example, differences in shape arise from optical differences between the center of the optical system and its edges. These cumulative effects can result in variation in delay of about 15%, and in variation in set-up and hold of about 15-20% depending on where the cell is placed. For standard-cell designers expecting nominal performance regardless of cell placement, the accumulation of these effects profoundly affects the ability to assure rapid time-to-volume with traditional methods.

These effects explain the growing tendency for "DRC clean" libraries and IP to be non-competitive, fail, or yield poorly in production. Design teams have little or no visibility into root causes of problems until post manufacturing analysis, adding millions of dollars in costs for diagnosis, repair and silicon respin. For 45nm designs, semiconductor designers need to establish methodologies that let them optimize libraries for specific manufacturing effects as well as for placement and routing. In particular, they need to establish methodologies to identify and prevent physical and electrical hot spots as early as possible in the design flow.

Semiconductor manufacturers are already applying Cadence advanced node methodologies to this type of cell optimization. Designers at leading electronics and foundry companies have used electrical DFM solutions from Cadence to analyze and optimize their cell libraries. In this approach shown in *Figure 3*, they have simulated the silicon shape (contours) from the drawn design, predicted the current of the transistor and the delta resistance/capacitance from these silicon shapes, extracted transistor parameters corresponding to this drawn current and performed timing analysis. In this flow, the Cadence Litho Physical Analyzer uses a fast, accurate, foundry-certified model to predict silicon contours. The model captures the entire RET/OPC manufacturing flow, including re-targeting, assist-feature insertion, PSM, and OPC information released by the designer-specific target fab. Another Cadence product, the Cadence Litho Electrical Analyzer, uses the design layout silicon contours and an existing circuit netlist to update the transistor parameters of the circuit netlist.

In one example, a semiconductor manufacturer—using a secure model for its proprietary process—ran Litho Physical Analyzer on a 100mm² full-chip CPU-core-based design, simulating contours of poly, active and metal layers across nine process window conditions overnight. After re-running statistical timing analysis with the SDF file produced by Litho Electrical Analyzer, the manufacturer's engineering team found additional critical paths that introduced marginality in the chip timing and required correction to avoid catastrophic failure.

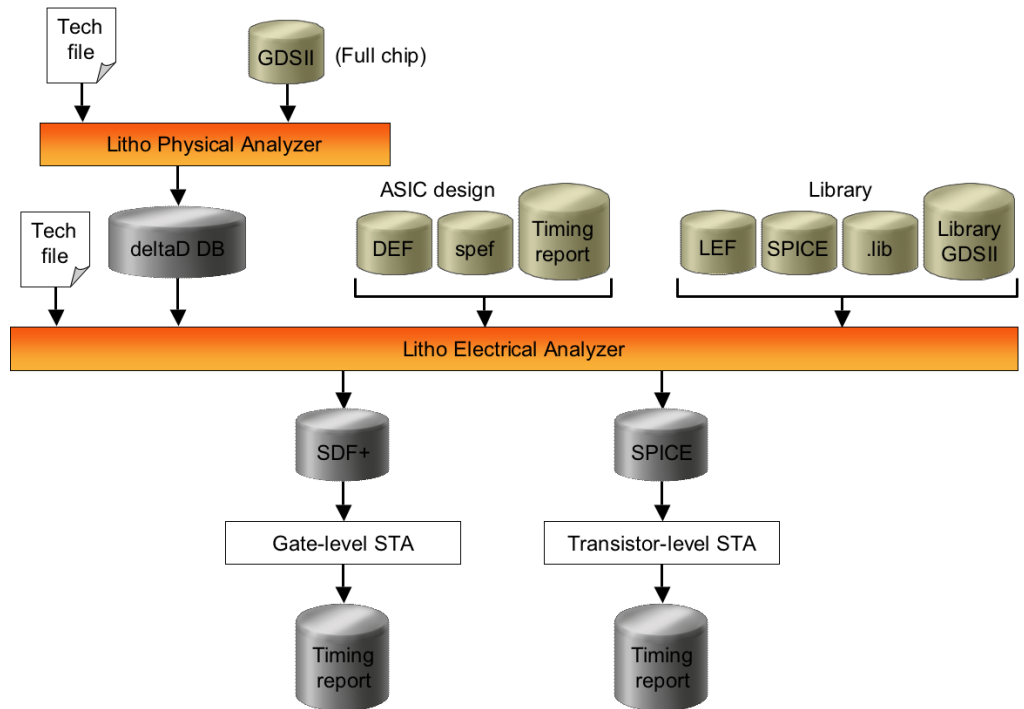


Figure 3. By using contour-based analysis of designs and extracting accurate values for use in static timing analysis, engineers can account for timing variations introduced by lithography.

WHAT ABOUT CUSTOM DESIGN?

For custom design—analog in particular—the growing impact of process variation and detrimental parasitic effects at advanced nodes have forced a new look at analog design methods. Analog engineers have typically relied on ensuring performance at the design corners as the standard for design sign-off. Yet, this approach offers no indication of yield or yield margin. Newer analog tools, such as the Cadence Virtuoso® Analog Design Environment GXL, address these issues directly. Virtuoso Analog Design Environment GXL can size a design automatically over all corners, and can also automatically adjust a design to maximize yield over all process variations.

Although parasitics are not a new concern for custom designers, advanced node technology significantly increases the total number of parasitic effects that engineers must now guard against. At sub-90nm design processes, it is not always possible to simply add many guard rings because they take up too much space. So, the designer is left to figure out how to build the design before layout to minimize waiting for the post-layout designs and extraction. By utilizing the parasitic re-simulation flow inside Virtuoso Analog Design Environment GXL, the designer is able to detect and prevent parasitics prior to layout. Knowledge gained from this work can be saved as part of the design IP so that when the block is re-used, the parasitic knowledge is known as well. This approach begins with the designer isolating the critical nets and determining maximum parasitic tolerances on those nets. Through a series of easy steps, those values can be determined and saved as "constraints" for those nets. Now, when the layout engineer either routes the net by hand or uses Cadence space-based routing technology, these constraints will help prevent route designs that can create signal integrity problems. Post-extraction, designers can use the same flow for analyzing secondary nets, or saving the parasitic data within the library so that the next time the IP is used, it has been well characterized.

Implementation problems go up exponentially due to the rule sets that must be followed to manufacture the design. A key component of implementation is routing. More advanced routing approaches such as the Cadence Space-Based Router are able to complete constraint-based layouts automatically or interactively. This constraint-driven design methodology lets designers tune physical designs based on performance or specialized structures. The capability is critical in optimizing designs in advanced processes with multiple metal layers dedicated to high-speed interconnect. Critical nets can be marked as such by logic designers for automatic routing on layers intended specifically for high-performance interconnects. This eliminates manual pre-routing tasks that in the past typically required months to complete for complex microprocessor designs.

With this approach, a physical design solution is implicitly "correct by construction," because each physical design decision occurs in the context of the constraints and design rules associated with each structure. Nevertheless, designers can override these guidelines when their experience tells them such a violation is needed to meet design or manufacturing objectives. By integrating the space-based routing technology under the Virtuoso platform cockpit, users can accomplish their most difficult routing tasks either interactively or by using the automated features contained within the router.

FASTER VERIFICATION FOR MORE COMPLEX DESIGNS

Traditional black-box approaches are no longer effective for emerging mixed-signal designs, which require longer simulation runs and more of them to achieve results needed to predict chip performance in the context of an advanced manufacturing process. Furthermore, the availability of a growing variety of mixed-signal implementation vehicles adds to growing pressures for more effective circuit simulation. Now, engineers must be able to deal effectively with designs implemented as single-chip analog ICs, mixed-single SoCs or silicon-in-package (SIP) devices. For optimal productivity, the circuit designer should be able to apply the same tools, methodology and models to each, avoiding any delays in dealing with different tool environments.

Cadence Virtuoso Spectre® Circuit Simulator with turbo technology allows designers to speed detailed verification of digital, analog and mixed-signal circuits as they explore IC architectures with no change in methodology or models using the industry-standard Spectre circuit simulator. This approach reduces analog design verification time with no sacrifice in accuracy, thereby improving design-cycle throughput and reducing costs. Virtuoso Spectre Circuit Simulator with turbo technology boosts simulation run times by 2 to 10X for pre-layout application circuits and 5 to 10X for post-layout, parasitic-dominant application circuits. Just as important, these speed advantages require no ramp-up time for engineers.

DESIGN-AWARE MANUFACTURING

Even as advanced node design must account for manufacturing effects early in design, manufacturing must ensure design objectives remain intact through mask preparation and silicon analysis. With the dramatic impact of advanced-node manufacturing on silicon performance, manufacturing cannot alter geometries in a physical design without awareness of the significance of those specific shapes on design performance. In sophisticated environments such as the Cadence Advanced Node Design solution, manufacturing tools rely on constraint data inserted throughout development to maintain design intent.

Newer tools take these capabilities to the next level through a growing array of automated mechanisms for correcting hot spots in physical designs. For example, Cadence optimization tools are able to read in data produced by lithography and CMP analysis tools and automatically fix hot spots in layouts. While the Cadence Chip Optimizer applies this technique with the metal layers in SoC designs, yield optimization technology in the Virtuoso platform applies these techniques to custom blocks.

In particular, this yield optimization technology works hierarchically to optimize utilization of “recommended” rules. Until now, designers have had few options in dealing effectively with recommended rule sets. With the explosion in rule deck size shown in *Figure 4*, custom design layout teams using traditional tools have faced a significant challenge in dealing with required rules alone. Consequently, layout engineers often create physical designs that simply ignore recommended rules, resulting in less than optimal yield. Alternatively, engineers might pick and choose a few recommended rules and consider them mandatory—an approach that typically sacrifices silicon area and performance. Other approaches provide only partial solutions, attempting to apply manual methods or simple DRC-based approaches to employ recommended rules in a few key standard cells. With the comprehensive Cadence yield optimization approach, designs achieve greater compliance with recommended rules than possible with these earlier approaches.

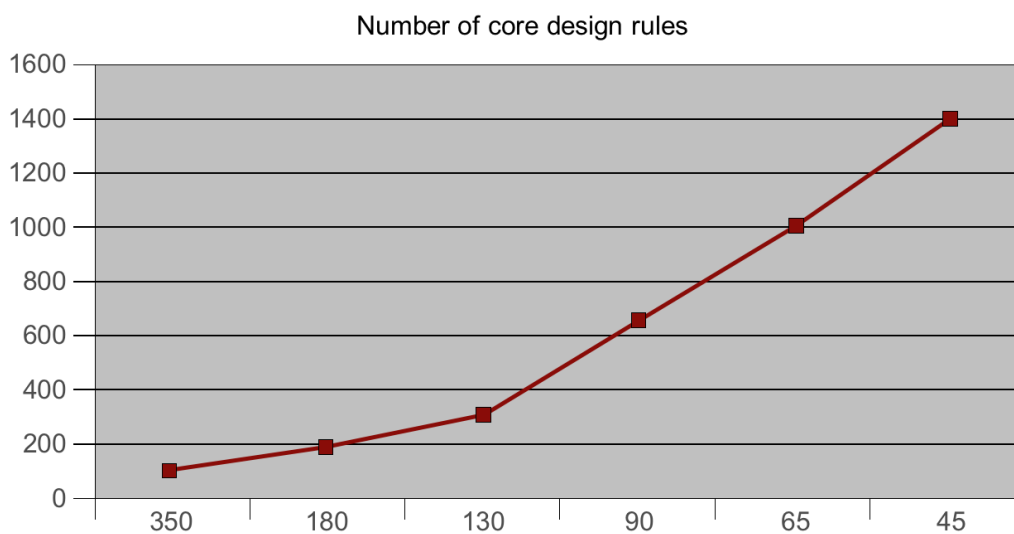



Figure 4. In order for fabs to print 45nm features using today's 193nm wavelength steppers, designers must follow more restrictive rules about the shapes and spacings they create during physical design.

FASTEST PATH FROM CONCEPT TO CONSUMER

As semiconductor companies look to exploit the advantages of 45nm technology, designers will face the growing impact of manufacturing effects on design performance. Integrated with the industry's leading custom and digital design flows, the Cadence Advanced Node Design solution offers an end-to-end approach that delivers concurrent signoff quality manufacturability analysis and implementation. Production-proven Cadence, model- and rule-based methods provide accurate results quickly and comprehensively, allowing designers to predict silicon performance more reliably despite the array of new effects that dramatically escalate the challenges of advanced-node IC design. The Cadence solution provides a complete design to manufacturing solution encompassing development, physical implementation, signoff and manufacturing. Using this environment, semiconductor companies can speed time-to-volume for complex advanced-node ICs.



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