



RF SIP DESIGN METHODOLOGY
AND FLOW



WHITE PAPER

OVERVIEW

System-in-package (SiP) design offers number of advantages over system-on-chip (SOC). Today, however, SiP is not scalable as a general design solution because it requires “expert engineering” talent in widely divergent fields. In order to move SiP implementation into the mainstream, companies need an integrated, scalable SiP environment and reference flow. Meeting this need will involve a radical change in design methodology for SiP products. Supported by a new technology, this methodology would enable engineers to co-design ICs, IC packages, and the targeted PCB, from concept to production.

This document describes the RF SiP reference flow that is an integral part of the Cadence® RF SiP Methodology Kit. The kit accelerates the application of advanced EDA technologies to system-in-package SiP designs for radio frequency (RF)/wireless applications, and enables complete RF and wireless front-to-back SiP design and implementation. It provides methodologies that maximize design productivity and predictability for customers leveraging the advantages of SiP implementation. Like all Cadence Kits, it addresses application-specific design issues by combining a verified methodology packaged in platform flows with enabling and standards-based IP—all applied to a segment representative design.

MARKET DEMANDS, TECHNICAL CHALLENGES

Manufacturers of wireless communication devices are increasingly turning to SiP design to help them squeeze more functionality into less space in a competitive time frame. One reason is that SiP implementation allows a high degree of flexibility in package architecture, particularly for RF applications. It also allows for lower power and less noise, flexibility in mixing and matching IC technologies. Additionally, relative to SoC, SiP modules can generally be created more quickly.

However, it is the advantage of SiP—the ability to incorporate combinations of digital ICs, logic ICs, RF ICs, passive components, and mechanical parts—that creates some of its greatest challenges. These challenges include the need for multi-technology simulation at the top-level, dedicated modeling techniques for integrated passives, and complex signal integrity and power delivery verification capabilities. The next-generation wireless systems promise to be even more complex as systems must be multi-standard and re-configurable.

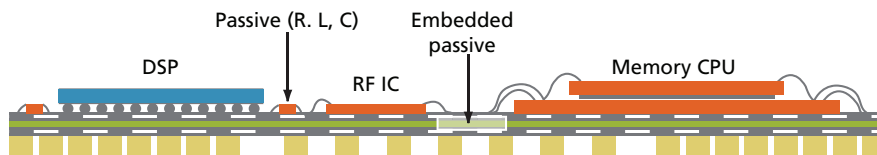


Figure 1: RF SiP example

RF SiP design is an integration and implementation platform based on a single package substrate that allows the integration of digital ICs, logic IC, and RF ICs plus passive components, SAW filters, and mechanical parts (Figure 1). In RF SiP design implementation, the package is no longer just a connectivity interposer between an IC and a board but has become the system integration vehicle and may contain many passive elements. This by itself makes an RF SiP very different from a typical digital SiP or IC package. For example, substrate interconnect/metal structures can be considered as critical devices which demand careful modeling and extraction and inclusion in functional circuit simulation so that high-order effects, such as dispersion and radiation, can be understood and managed.

THE RF SiP DESIGN CHALLENGE

The focus of this section is on the key RF design challenges that will have significant impact on the design tools, methods, and flows for integrating RF systems in SiPs.

RF SiP modules are made up of multiple design components of various technologies integrated into a common package. This means that for successful implementation, designers require a comprehensive simulation solution for analog, mixed-signal, RF, and full-chip design verification as well as multi-technology support for simulating dies from different process technologies together at the top-level system. Managing concurrent simulation of two disparate technology die is further compounded by the fact that the RF SiP module substrate is based on yet another, completely different process technology.

RF adds more complexity due to the high-frequency nature of designs. RF design requires specialized and unique analysis techniques. Time-domain and frequency-domain are theoretically a duality, but as a practical matter, SiP requires merging these domains. The methods designers choose depend on the basis of circuit type, designer comfort level, circuit size, or designer preference. Ultimately, this requires a seamless environment that facilitates choice in simulation method.

In contrast to analog and custom digital simulators, FastSPICE simulators are not as practical when simulating RF effects across the board. To speed simulation, designers may use envelope-based analysis, which accelerates simulation of circuits that have a combination of very high and low frequency signals.

RF systems are highly dependent upon passive components for matching, tuning, filtering, and biasing. High Q and tight tolerance inductors and capacitors are especially prevalent in wireless systems and, as off-chip components, add cost in both real estate and assembly. Passive integration is a key component for system miniaturization and cost reduction. Two types of integration technologies are used for RF SiP applications: integrated passive devices (or networks) and embedded passives.

Integrated passive devices are typically glass, GaAs, or silicon thin-film solutions interfaced to the SiP like other chip devices through wirebond or flip-chip technologies. Embedded passive technology integrates the passive device into the RF SiP substrate in the same way spiral inductors and inter-digital capacitors are integrated. In comparison to integrated resistors and capacitors, spiral inductors require dedicated synthesis and analysis capabilities in addition to parameterized layout cells. Designers may need to use a field solver to capture coupling effects between single inductors and/or between closely spaced interconnects during a post-layout extraction.

Other effects of physical design can have a greater impact on RF circuits than those found in analog design, typically requiring RF designers to include accurate models of the system interconnects during simulation. For critical parts or 3D structures like bond wires, electromagnetic simulations may be required to capture S-Parameters for accurate simulations. In addition, high-speed requirements make RF circuits extremely sensitive to signal and power integrity issues.

Due to the lower device count, layout automation is less of a concern in RF design, although connectivity-based, constraint-driven layout and device generation enhances productivity. The RF domain is highly sensitive to physical topologies. As a result, these topologies generally require a large number of iterations between layout, extraction, and circuit design. In light of this, optimization of an RF circuit becomes a tedious process. A constraint-driven flow will ensure that the designer's intent is captured and will shorten the cycle.

Integration of the various portions is usually performed at the latter stage of the design cycle. Design errors caused by misinterpretation of specifications (usually due to ambiguous language), improper interface connections, etc., become very expensive when detected at this late stage.

Thus, the essence of the RF SiP flow is the ability to manage, replicate, and control post-layout simulations and effects and to effectively use this information in a timely fashion at appropriate points throughout the design process.

In summary, RF SiP challenges need to be addressed by a complete solution that:

- Provides a seamless flow starting at full SiP electrical simulation, continuing through a single schematic-driven layout implementation, and ending with comprehensive signal integrity checks
- Achieves functional, performance, and closed-loop verification across multiple technologies and design domains including system-level, digital, mixed-signal, and analog/RF
- Improves simulation accuracy and completeness by effectively combining signal integrity analysis at SiP level and parasitic extraction at IC level
- Optimizes on- and off-chip configurations by managing inductor synthesis and passive component modeling

All of the above requirements must be met through a common environment, which not only facilitates the job of the SiP designer natively, but also integrates with IC and physical package implementation. This must include both SiP- and chip-level perspectives at multiple abstraction levels, where the same design collateral can be passed back and forth facilitating verification/implementation from either environment point of view.

AN IDEAL RF SiP FLOW

The solution comes in the form of a change in the design methodology for SiP products. A co-design environment that accommodates the RF IC flow and links this schematic-based flow to package implementation is a core requirement in addressing RF SiP design challenges.

Co-design brings a model of all design domains (IC, package, and board) into a common design environment that allows global optimization and characterization of the design in development, starting at the top-level electrical simulation of the entire system or sub-system. It is a design process that manages the physical, electrical, and manufacturing interfaces between design components across all of the associated design domains. It is the only way to reconcile aggressive time-to-market demands, complex cost structures, and tradeoffs in system architecture.

Collaboration across the design chain must be facilitated because effective SiP design will involve a complex design chain of system, SoC, circuit, package, and board designers. Traditionally, these designers have worked independently and designs have been created, simulated, implemented, and verified separately using different tools, methods, and flows, often without a single system-level circuit simulation view of the entire design. At integration, special attention needs to be paid to who will be running the top-level simulations and performing top-level physical design and from where design collateral (netlists, models, databases, etc.) will come. Design collateral is an important part of an effective integration across design domains. In SiP design, a designer must not only consider that a block meets specification but also what (and how) design collateral will be used to support both integration and a fast design process—particularly at the top level. This collateral needs to be natural fallout of the design process in each design domain.

A new, single mega-environment for RF SiP is not the answer—an RF SiP design solution needs to integrate with existing IC design tools and flows. For an RF SiP solution to be used effectively, it must be a natural part of the environment a particular engineer is using.

The best place to start defining an RF SiP design flow is from a global methodology perspective and context. Engineers need an encompassing methodology that enables them to focus on their areas of expertise, verify their designs in a system-level context, and integrate their IP at the top level. In the IC domain, there are two different flows depending on the application—a schematic-based custom (or full-custom) IC flow for RF/analog/mixed-signal front-to-back IC implementation and a digital implementation flow. So for RF SiP design, the target approach needs to come from a custom point of view, where the underlying methodology is based on an Advanced Custom Design (ACD) methodology. The ACD methodology is primarily focused on IC design but is applicable to a variety of integration strategies.

The ACD methodology defines a process geared towards mixed-technology design, which takes design tasks and parallelizes them—allowing for a top-level perspective—for parasitic and analysis functions performed early and often. It ultimately enables the design to progress with as much information as is available at any given point in time. Predictability is the driving force behind the ACD methodology.

The need for predictability is driven by two primary concerns: the schedule, which must be met from the beginning of the design process and which necessitates a fast path to manufacturing, and performance requirements, which must be met to achieve first-pass success and which require a system interconnect-accurate methodology.

In order to address the challenges for RF SiP design as outlined in the previous section, a simple incremental growth in features and capabilities in packaging tools is not sufficient to meet the challenges. As mentioned before, a SiP solution needs to tie together the IC world for front-end design and the package world for the physical implementation of the SiP.

Figure 2 shows the major building blocks of the RF SiP task flow. The flow starts when a system implementation concept has been defined and the system architecture has been partitioned into a set of components that will be integrated to form the system.

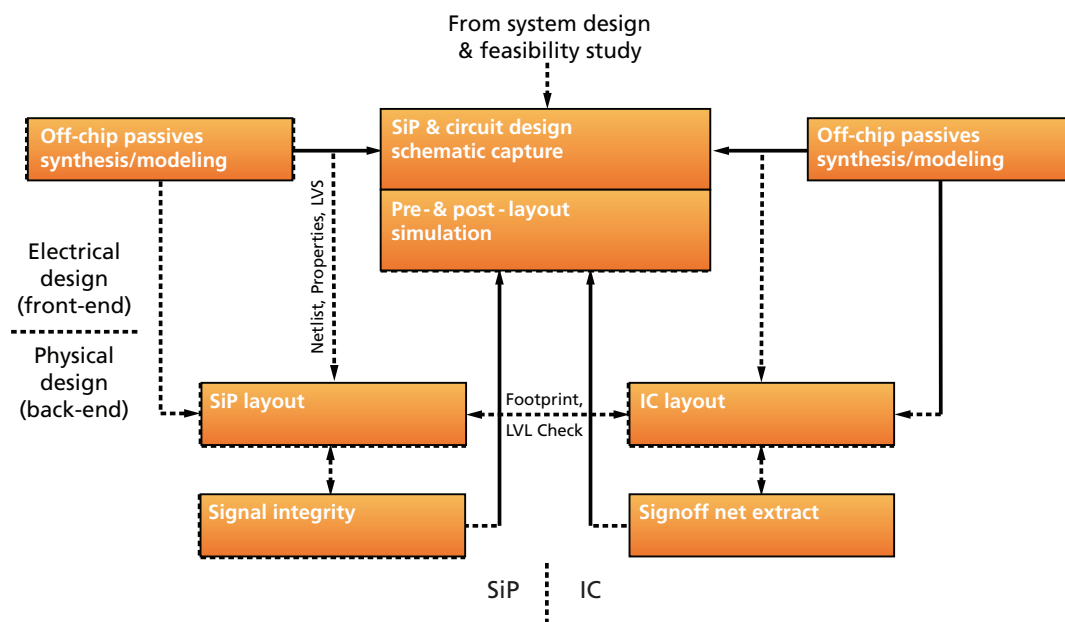


Figure 2: RF SiP task flow

The task flow diagram can be distinguished as four main areas. The top of the diagram addresses the front-end (schematic entry and electrical simulation) and the bottom represents the back-end (physical design and extraction) of the flow. The left side captures the SiP and the right side the IC tasks.

The following description of the flow will focus on the SiP part of the flow; the IC part is only shown for reference to describe where and how it interacts with the SiP flow. Details on the RF IC flow can be found in The RF Design Methodology Kit White Paper.

PRELIMINARY SCHEMATIC AND TEST BENCH SETUP

The top-down process starts with a preliminary circuit design, where a high-level schematic is assembled to study the feasibility of the design and verify overall system performance. At this stage, transistor-level or detailed models of all subcomponents may not yet exist. Therefore, the designer will have to use behavioral or other high-level modeling techniques to represent the missing parts. This allows for exploration of various implementation alternatives and for short verification cycles. Typically, ideal elements are used to represent the off the shelf SMD components and substrate embedded passive components. Also top-down Verilog-A, Verilog-AMS, or VHDL models will be used to represent the functionality of the large mixed-signal and digital ICs. RF and high-speed circuits may also include estimates of interconnect parasitics and transmission line effects.

Simulation setups are created and kept in the design environment, which enables effective management of numerous simulations and views of each block. Later, during implementation, the full simulation environment will be comprised of several views of the same circuit. These are likely to include a behavioral view, a pre-layout view, several views of parasitic information (one view may hold a lumped-element RLC subcircuit, one view an S-Parameter representation created by field solver, etc.), and perhaps a backannotated behavioral view.

This full-SiP setup serves as an executable specification to enable continuous verification as blocks mature, creating a continuous evolutionary approach through the entire electrical and physical design process. This is important because problems can be detected at the earliest stage possible, while time still remains to fix them, and because blocks can be designed in parallel according to individual schedules. These specifications will then be used to control the implementation process of each component and its integration into the SiP design.

DETAILED SCHEMATIC

After the early design explorations, the next step involves mapping ideal components to physical implementation options (e.g. embedded vs. SMD). This requires the synthesis of passive components such as spiral inductors, transmission line elements, and inter-digital capacitors to specification. This process delivers two key outcomes: the creation of early models for passive components that can be used in simulation before the block-level layouts are complete and parameterized layout representations (pcell) that can be used for the physical implementation in the targeted process. This also enables the initial analysis of mutual coupling such as between spiral inductors.

It is important to note that the complete SiP design, including the on-chip circuitry of the various die, will be captured in a single schematic stored in a single database. The environment will also support a schematic-driven layout implementation that is connectivity-correct and propagates constraints from the schematic to the layout representation. Layout versus schematic (LVS) checks, component cross-probing between schematic and layout, and backannotation of parameter changes in the layout into the schematic and vice versa are further key requirements enabled through the flow.

PRELIMINARY SiP PLACEMENT AND FLOORPLAN

At some point, the design will be mature enough to begin the physical layout implementation. This should be done early in the design cycle as a way of determining the optimal package floorplan to reduce size and cost, and to determine the best technology partitioning and I/O placement. All components, including the automatically created IC die footprint symbols, embedded pcell components, etc are placed in the design. Support for both flip-chip and wire-bond die attach options are further required at this point.

Layout automation (automated routing, connectivity-driven layout, constraint-driven layout, and placement) can be used judiciously. There are two advantages of using layout automation—it is tied to the schematic and it enables productivity gains. In the forward direction, the schematic information is passed directly to the layout editor. While any changes made during the layout design phase can be annotated back to the schematic. In this way, both the schematic and layout can remain synchronized. This enables a physical design process that can become just as repeatable as the front-end process. The time and overhead expended to setup the initial tools is more than compensated for by reductions in the number of iterations through the design process. Engineering change orders (ECOs) are also performed more effectively if a repeatable layout process is in place. The repeatability of an automated layout process is weighed against the requirements of highly sensitive circuitry, which demands a manual approach.


CREATE SiP LAYOUT

After the initial SiP substrate feasibility, creation of the floorplan adding the interconnect routing completes the electrical portion of the physical design flow. Flight lines indicating the un-routed nets may be used to guide the manual detailed routing process that is normally used for the critical RF signal nets. Often these nets have a combination of impedance and routing constraints that prevent usage of automatic routers. Therefore, these nets are typically given preferential treatment and routed first followed by critical power and ground connections. Finally, the remaining signal and power nets are added. At this point, complete design-rule (DRC), LVS, and layout versus layout (LVL) checking needs to be done. For complex SiP designs 3D visualization checks are also desirable.

POST-LAYOUT EXTRACTION AND RE-SIMULATION

RF SiP design is highly sensitive to parasitic effects. As the physical RF SiP substrate layout is implemented, EM simulation most likely needs to be used to provide highly accurate models for passive components and the interconnection path for critical signals. For example, several spiral inductors along with the surrounding interconnects may be selected as highly critical and a target for EM simulation. These EM simulation models can be swapped to replace the models that were created early in the design process and can be mixed and matched with existing models. The ability to manage different levels of parasitic information is paramount. The ability to describe the amount of parasitic information to be included for each area, line, or block enables the designer to trade off simulation runtime versus accuracy.

Managing drawn inductors through the parasitic extraction process is an important aspect of a complete design flow and warrants special consideration. In fact, one can consider inductor creation to follow the meet-in-the-middle methodology. Early in the design process, these inductors are drawn (or synthesized) using a top-down model. As the design progresses, and as layouts mature, the bottom-up process enables more refinement. At this bottom-up stage, full parasitic effects are included for the inductor as well as the surrounding circuitry using the same parasitic methodology as the rest of the circuit. This enables more accurate representation of these critical components.



Circuit designers need the ability to choose the method most appropriate in the up-front process: a fast, quasi-static 3D EM solver or a slower, but more accurate 2.5-3D EM full-wave numerical solver. The full-wave EM solutions are better for complex shapes and higher-frequency harmonics while the quasi-static approach is superior for large coupled areas of the design. But all circuits do not have these needs. An important element of the flow is the efficient backannotation of the extracted model or S-Parameters data file to the schematic for a parasitic re-simulation. As an example, critical interconnect structures in the SiP layout might be synthesized into discrete transmission line elements and backannotated into the schematic. The full parasitic check at the end serves as the signoff.

SUMMARY

The RF SiP implementation methodology provides a new packaging platform with the advantages of high flexibility, lower cost, and faster cycle time than SoC implementations. SiP technology enables integration of digital and logic ICs, RF ICs, and passives into a single package in a cost-effective process.

The lack of a complete design flow including design tool interaction between design domains and an underlying methodology has been identified as a key requirement to fully leverage the advantages SiP offers. Many companies will be able to remove weeks or months from their RF product design process through the combination of best practices and the deployment of the proposed co-design methodology and associated technology platform. These best practices, and the proposed co-design methodology and associated technology platform, all applied to a segment representative design, are the basis for the Cadence RF SiP Methodology Kit.



For more information,
log on to www.cadence.com

cādence™

Cadence Design Systems, Inc.

Corporate Headquarters
2655 Seely Avenue
San Jose, CA 95134
800.746.6223 / 408.943.1234
www.cadence.com