CREATING LOW-POWER DIGITAL INTEGRATED CIRCUITS – THE IMPLEMENTATION PHASE
**INTRODUCTION**

Power consumption has now moved to the forefront of digital integrated circuit (IC) development concerns. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Furthermore, with every new process generation, leakage power consumption increases at an exponential rate.

In recent years, a wide variety of techniques have been developed to address the various aspects of the power problem and to meet ever more aggressive power specifications. These techniques include clock gating, multi-switching threshold (multi-Vt) transistors, multi-supply multi-voltage (MSMV), substrate biasing, dynamic voltage and frequency scaling (DVFS), and power shut-off (PSO). Figure 1 illustrates the power, timing, and area tradeoffs among the various power management techniques.

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<tr>
<th>Power-reduction Technique</th>
<th>Power Benefit</th>
<th>Timing Penalty</th>
<th>Area Penalty</th>
<th>Methodology Impact</th>
<th>Architecture</th>
<th>Design</th>
<th>Verification</th>
<th>Implementation</th>
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<tbody>
<tr>
<td>Multi-Vt Optimization</td>
<td>Medium</td>
<td>Little</td>
<td>Little</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>None</td>
<td>Low</td>
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<tr>
<td>Clock Gating</td>
<td>Medium</td>
<td>Little</td>
<td>Little</td>
<td>Low</td>
<td>Medium</td>
<td>Low</td>
<td>None</td>
<td>Low</td>
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<tr>
<td>Multi-supply Voltage</td>
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<td>Little</td>
<td>High</td>
<td>Medium</td>
<td>High</td>
<td>High</td>
<td>Medium</td>
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<tr>
<td>Power Shut-off</td>
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<td>Some</td>
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<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
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<tr>
<td>Dynamic and Adaptive Voltage Frequency Scaling</td>
<td>Large</td>
<td>Some</td>
<td>Some</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
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<tr>
<td>Substrate Biasing</td>
<td>Large</td>
<td>Some</td>
<td>Some</td>
<td>Medium</td>
<td>None</td>
<td>None</td>
<td>High</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1. Tradeoffs associated with the various power management techniques

Notably, designers cannot simply “bolt on” low power” at the end of the development process. The size and complexity of today’s ICs makes it imperative to consider power throughout the design phases—the chip/system architecture, power architecture, and design (including micro-architecture decisions)—and all the way to implementation with power-aware synthesis, placement, and routing. Similarly, in order to prevent functional issues from surfacing in the final silicon, power-aware verification must be performed throughout the development process.

The various aspects of the power-aware development process may be summarized as follows:

- **Chip/System Architectural Specification**: Power-aware design starts with the architectural specification of the chip/system, including partitioning the system into its hardware and software components. At this stage, evaluations should be made as to which blocks are not performance-critical, which means they can potentially be run at a lower voltage and/or frequency to conserve power. Similarly, certain blocks may be suitable candidates for “sleep mode” or to be completely shut down to conserve power when they are inactive.

- **Power Architecture**: Following the definition of the chip/system architectural specification, the next step in the development process is to refine the power architecture. For example, the architectural specification may specify that a certain block should be implemented in such a way that it is capable of being completely powered down. In the power architecture portion of the process, the team will determine just how often this block is to be shut down, and also any interdependencies among this block and other blocks and modes.
• **Power-Aware Design:** In this context, “design” refers to the portion of the flow where – taking the results from the chip/system architecture and power architecture phases – design engineers capture the RTL descriptions for the various blocks forming the design. The designers associated with each block are responsible for ensuring that the block will meet its functional, timing, and power requirements while occupying the minimum silicon real estate.

• **Power-Aware Implementation:** The implementation phase is where all of the work performed during the chip/system architecture, power architecture, and power-aware design phases comes to fruition with the aid of power-aware engines for logic synthesis, clock gating, placement, clock-tree synthesis, routing, and so forth. In addition, during the implementation phase, the logical and physical structures needed for the various power techniques are created. These include power grid synthesis, power plane implementation, and insertion of level shifters, switch cells, isolation cells, and state-retention cells.

• **Power-Aware Verification:** Verification commences with the planning process. Every hardware and software element comprising the design that is to be tested is detailed, the way in which each element will be verified is defined, and the required coverage metrics for each element are specified. In a modern design environment, verification planning must be complemented by a sophisticated verification management functionality that interprets the plan and automatically deploys the appropriate tools required to perform comprehensive verification.

Each of the above topics is introduced in more detail in a companion whitepaper titled: “Architecting, Designing, Implementing, and Verifying Low-Power Digital Integrated Circuits”. The remainder of this paper focuses on the power-aware implementation portion of the development process.

**POWER-AWARE IMPLEMENTATION**

A wide variety of decisions will have been made during the Chip/System Architecture, Power Architecture, and Power-Aware Design portions of the design flow. These decisions typically involve the use of multiple power-saving technologies and techniques, such as:

- Clock gating
- Multi-switching threshold (multi-Vt) transistors
- Multi-supply multi-voltage (MSMV)
- Power shut-off (PSO)
- Substrate biasing
- Dynamic voltage and frequency scaling (DVFS)
- Selecting the appropriate on-chip interconnect mechanism, such as a globally asynchronous locally synchronous (GALS) architecture.

The Power-Aware Implementation phase is where these decisions come to fruition and are made real.
COMMON POWER FORMAT

A key enabler of a modern power-aware design flow is the ability to capture and preserve the intent of the chip architects and designers throughout the design flow. This requires a common specification format that can be used and shared across the entire design chain, from architectural specification (“this block has three power modes”) to verification (“will the chip recover if these blocks are put to sleep in this order?”).

The current state-of-the-art with regard to such a specification is the Common Power Format (CPF), which is managed under the auspices of the Silicon Integration Initiative (Si2) consortium’s Low Power Coalition. CPF is a new format that enables design teams to capture the intent of a design from a power perspective. It provides a mechanism to capture architects’ and designers’ concepts and constraints for power management, and it enables the automation of advanced low-power design techniques. CPF allows all design, implementation, verification, and technology-related power objectives to be captured in a single file and then applies that data across the design flow, thereby providing a consistent reference point for design verification and implementation.

Using CPF to drive the design, verification, and implementation steps of the development flow helps to:

• Achieve the required chip specs by driving the implementation to match the required design architecture
• Integrate and automate the design flow, which increases designer productivity and improves the cycle time
• Eliminate the need for manual intervention and replaces ad hoc verification methodologies, thereby reducing the risk of silicon failure due to inadequate functional or structural verification.

TOP-DOWN MULTI-DIMENSIONAL OPTIMIZATION

One key requirement for low-power design is the ability of logic and physical synthesis engines to concurrently optimize for timing, area, and power tradeoffs. For example, by replacing nominal-Vt cells with high-Vt cells, optimization engines can reduce power at the expense of performance. However, power should not be an afterthought to the optimization process where first the timing targets are achieved and later on cell swapping is done to reduce power. This means that—starting with the logic synthesis stage and extending all the way to routing—the optimization engines need to create structures that can meet performance targets while minimizing power consumption.

Similarly, in the case of MSMV designs it is important that the optimization engines understand power domains top-down so that they have full visibility to optimize across entire timing paths. Using a top-down optimization approach for MSMV designs leads to superior timing, area, and power tradeoffs. Furthermore, the ability to explore power-timing tradeoffs at the topmost level eliminates the need for multiple iterations that are common in bottom-up partitioning.

POWER GRID IMPLEMENTATION AND ANALYSIS

Power domains must be shaped and placed; power pads and switches must be placed and optimized; and power routing must be planned. Silicon virtual prototyping helps the partitioning process by minimizing the wire lengths of any high switching probability wires, which lowers the dynamic power. This requires tools that are not only able to understand which wires contribute the most capacitance but also to find ways to minimize the interconnect capacitance through optimal partitioning and floorplanning.
The robustness of a design’s power networks has a direct impact on its performance. Voltage (IR) drops on VDD nets and ground bounce on VSS nets affect a design’s overall timing and functionality and—if ignored—can cause silicon failure. High currents in the power grids also induce electromigration (EM) effects, causing the power routing to wear out (i.e., to become more resistive) during a chip’s lifetime.

A complete picture of power grid robustness can only be obtained when effects such as IR drop, ground bounce, and EM are accurately computed and analyzed. These are full-chip issues that must be addressed by verification tools that have the capacity and performance required to analyze detailed representations of the entire chip in a reasonable amount of time.

Timing, signal integrity, and power analysis should be performed with the effects of IR drop and ground bounce included once the power grid is routed. By analyzing and verifying power grids, timing, and signal integrity at the full-chip level, designs can be taped-out with high level of confidence in achieving first silicon success.

CLOCK-GATING CHALLENGES

Though clock gating has been used for some time as an effective technique to reduce dynamic power, today’s stringent power specs demand ever more sophisticated gating techniques. The most sophisticated form of clock gating currently available is multi-stage gating, in which a common enable is split into multiple sub-enables that are active at different times and/or under different operating modes. And, of course, the process is further complicated when it comes to clock trees that pass through different power domains, especially when one or more of those power domains are candidates for power shut-off.

PHYSICAL IMPLEMENTATION OF LOW-POWER STRUCTURES

Multiple power domains in MSMV and PSO techniques require the insertion, placement, and connection of specialized power structures, such as level shifters, power pads, switch cells, isolation cells, and state-retention cells.

In particular, PSO requires a special (and more complex) set of considerations for implementation and analysis. For example, one of the considerations on the implementation side is that designers need to make a tradeoff between using fine- and coarse-grained power gating. Fine-grained gating includes a power-gating transistor in every standard cell, which has a large area penalty but eases implementation. Coarse-grained gating reduces the area penalty by using a single gate to cut off power to an entire block, but requires sophisticated analysis to determine the gating current of the switched-off block. On the analysis side, designers must consider the impact of powering up several blocks at the same time, which could lead to IR drop in the adjacent circuitry caused by the large rush currents associated with power-up. This requires dynamic power analysis to better understand the power-up characteristics with a goal of reducing rush currents and minimizing IR drop impact.
SIGNAL INTEGRITY CONSIDERATIONS

With increasing clock frequency and the lowering of supply voltages comes increasing sensitivity to signal integrity (SI) effects such as crosstalk-induced delay changes and functional failures. Furthermore, the use of advanced power management techniques makes SI analysis even more complicated. In the case of a PSO design, for example, a spurious signal caused by an SI aggressor could shut down an entire module. Similarly, the use of multiple power domains can lead to the creation of super-aggressors, where victim nets in a low-voltage domain can be weaker and aggressor nets in a high-voltage domain can be stronger. Overall, multi-Vt, MSV, and PSO techniques require implementation and analysis tools to be power-aware so they can account for these SI effects.

LOW-POWER FORMAL VERIFICATION

Low-power designs may fail due to a number of structural errors, such as missing level-shifters/isolation logic, redundant level-shifters/isolation cells, bad power-switch connections, and bad power and ground connections. Some possible functional errors include bad state-retention sleep/wake sequences and bad logic for power gating and isolation. Thus, it is important that designers use robust formal verification techniques to identify and rectify these structural and functional errors.

POWER ANALYSIS

Power analysis, like timing analysis, needs to be consistent and convergent throughout a design flow. Early power analysis that is not implementation-aware will fail to have any insight into what types of timing, area, and power optimizations that will be required to meet the design’s constraints. This amounts to no better than a guess. Unrealistic early power estimation can have serious negative effects, such as causing cost overruns due to a more expensive package, pursuing the wrong architecture or optimization strategy, or schedule overruns.

Throughout the implementation flow, power analysis needs to accurately calculate and report all components of power consumption, including active power and leakage power. Power analysis also requires comprehensive reporting that enables designers to understand where power is consumed and how it could be minimized. A good design flow should employ consistent power calculations that use the best available implementation insight from early power estimates through sign-off power calculation, so that power is constantly measured, refined, and properly acted upon.

POWER RAIL ANALYSIS

Power rail analysis should be performed early in the design flow to ensure robust power grids from time zero. Power switches and de-coupling capacitance must be optimized using power rail analysis to ensure that margin-driven over-design is limited. As the design progresses, power rail analysis should be used to continuously validate that the on-chip power delivery is still within specification as the design becomes complete.

Power rail sign-off verification demands a hierarchical, full-chip solution that delivers the capacity and performance required to analyze detailed representations of the entire chip in a reasonable amount of time. Timing, signal integrity, and power analysis should be performed with the effects of IR drop and ground bounce included once the power grid is routed. By analyzing and verifying power grids, timing, and signal integrity at the full-chip level, designs can be taped-out with high level of confidence in achieving first silicon success.
HOLISTIC POWER-AWARE IMPLEMENTATION

A major consideration in low-power design is to ensure that each power-centric implementation technique is executed in a holistic manner, taking account of all of the other techniques being employed on a particular design. Each technique has to be supportive of the other techniques, and any power savings achieved from one technique need to be maintained and preserved by the other techniques. For example, one of the most basic savings in power is to not use the biggest drivers. A slight reduction in margins will result in a smaller design occupying less area and consuming less power. But if the design environment does not support power-aware timing closure, it may negate any power savings achieved earlier in the process by adding too many cells for delay fixing.

Similarly, the practice of adding extra timing margin to account for arbitrarily set amounts of IR drop will negatively impact power consumption. Thus, once again, it is important that all optimization techniques simultaneously consider all of the implementation objectives to achieve the best possible solution.

Use of the Common Power Format (CPF) is the key to effective power-aware implementation. The CPF captures the intent of chip architects and designers and enables automatic optimizations throughout the design flow. Of particular interest is the fact that having this specification separate from RTL enables re-use of a block in different power profiles.

By employing automation tools that understand the designer’s power intent through CPF for optimization, design planning, and layout steps, design teams can achieve superior timing and power tradeoff while improving the productivity and cycle time during the implementation phase.

SUMMARY

Design teams across the semiconductor industry are adopting power management techniques to meet their market-driven low power requirements. In addition to the usual considerations of chip performance, functionality, and cost, these new power-related requirements include improved battery life, reduced system cost, cooler operation, and improved reliability.

Although advanced low-power techniques such as MSMV, PSO, and DVFS can be used to manage power consumption, these techniques have profound impact on the chip design, verification, and implementation methodologies. Often, the complexities associated with these advanced techniques result in low-power designs that suffer from sub-optimal timing, power, and area tradeoffs; reduced productivity and turnaround time; and increased risk of silicon failure.

To enable the adoption of advanced low-power techniques by mainstream users, there is a need for a design flow that holistically addresses the architecture, design, verification, and implementation of low-power designs. The Common Power Format (CPF) has emerged as an effective means to capture the design’s power intent early on and to communicate this intent throughout the design flow.

A key requirement for today’s low-power design is for the physical synthesis engines to have the ability to concurrently optimize for timing, area, and power tradeoffs. By analyzing and verifying power grids, timing, and signal integrity at the full-chip level, designs can be taped-out with high level of confidence in achieving first silicon success.
Power-aware implementation requires concurrent implementation and analysis that includes power-aware placement-and-routing, careful attention to how clocks and signals pass through multiple power domains, and correct physical implementation accounting for multiple supply voltages. Power-aware implementation also needs to manage the physical implementation of special low-power elements (such as level shifters, power switches, and isolation cells) that are necessary to successfully create low-power layout.

Low-power design methodologies are understandably becoming more complex, which causes a barrier to adoption. To ease the adoption challenges, comprehensive information, instruction, and documentation are required. One solution comes in the form of design kits, which contain such information and enable expert and non-expert teams to rapidly adopt advanced low-power techniques efficiently and effectively.

Last but not least, pre-tapeout timing sign-off requires concurrent analysis that includes the effects of IR drop and the validation of multiple modes of operation. Failure to comprehensively account for all influencers of timing during sign-off increases the risk of silicon failure and design re-spin.

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