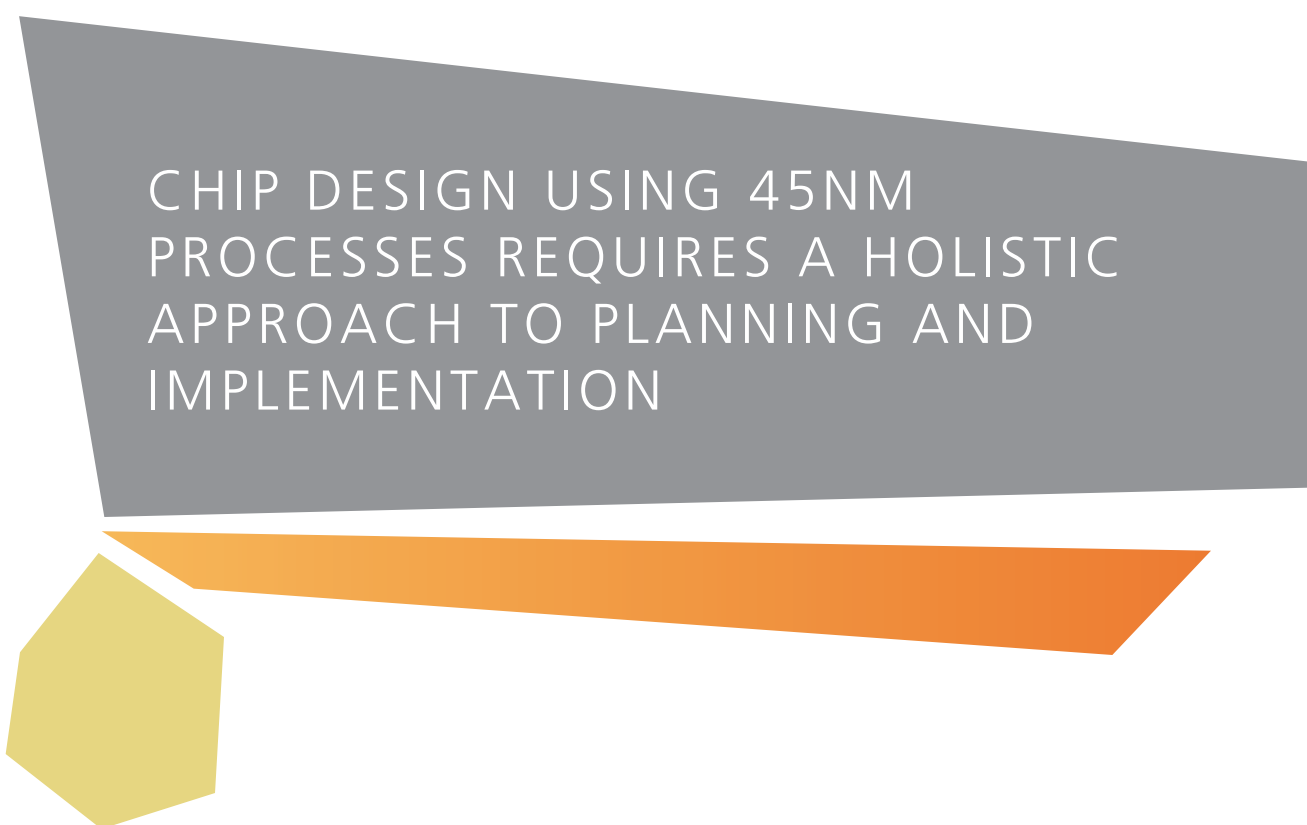




# WHITE PAPER



CHIP DESIGN USING 45NM  
PROCESSES REQUIRES A HOLISTIC  
APPROACH TO PLANNING AND  
IMPLEMENTATION

ERICA BRAND

The persistent push to shrinking process nodes continues, with many designs today manufactured using 45nm processes. Smaller process nodes are used primarily to reduce the area, thus the cost, of chips. For forty years, the decreased transistor and wire sizes also brought increased speed and reduced power consumption, but those benefits have declined as the devices approach atomic limits. The targeted gain in transistor density is accompanied by challenges of leakage, power management, timing predictability, and line printing fidelity for devices at these small dimensions. Recent ultra-conservative, restrictive design rules prevent layout from shrinking even as the gate length does. Both the physics of miniature devices and the available manufacturing methods require that the chip designers perform up-front planning and trade-offs to achieve manufacturing success. For example, voltage scaling has plateaued as a power reduction technique, and while high-k gates greatly reduce leakage power, architectural-level power management planning is required to reduce overall power consumption. (see *Figure 1*)

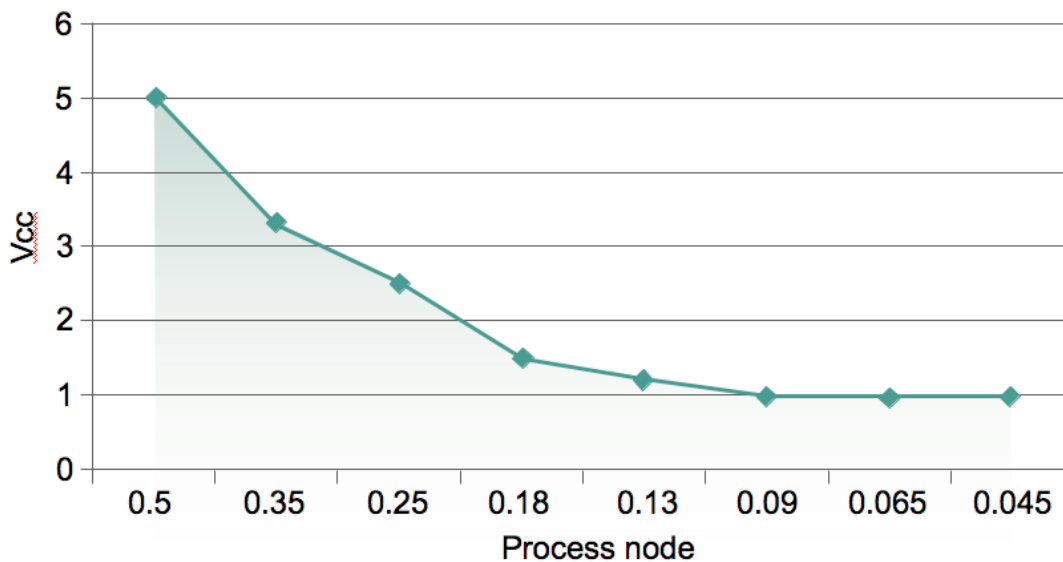


Figure 1: Voltage scaling plateaus below 130nm

Designing chips in 45nm processes requires more planning, extra analysis, and complex trade-offs to reduce die area while maintaining or gaining performance, yield, and reliability. In addition, the high cost of fabs and corresponding consolidation of manufacturing to a few companies means chip designers must achieve product differentiation through design rather than manufacturing. The results are that more of the burden of a chip's success falls on the designers, and that all facets that contribute to that success—functionality, power, manufacturability—need to be incorporated into the design from the start.

Many of the challenges chip designers face when targeting 45nm process nodes fall into the two categories of manufacturability, and scale and complexity. While less aggressive designers leverage predefined blocks of proven-manufacturable layout to achieve yield with fewer iterations, they must still face the scale and complexity issues in today's designs. Chip designers can tackle these challenges most effectively through an integrated, holistic approach that enables consistent inclusion of manufacturing data and delivers productivity gains for the entire chip design flow.

## MANUFACTURABILITY

At 45nm, devices are scaled to less than 100 silicon atoms along the channel length, less than 1000 dopant atoms in the active area, and only a few atomic layers of insulating oxide. Key new technologies for manufacturing at 45nm include aggressive use of lattice strain, high-k gate insulators, laser annealing, and extremely low-k interconnect dielectric. As device dimensions approach atomic limits, variability effects are magnified and new design methodologies, used selectively on 90nm and 65nm designs, are increasingly valuable to gain control and predictable results at 45nm. For example, lattice strain techniques used in 45nm processes contribute to variability that even the layout designer cannot mitigate. Traditional simulation and timing analysis steps use more process corners to find vulnerable circuits but take more time and computation. Newer statistical methods save time and reduce guardbanding to help create chips that can take advantage of 45nm performance improvements.

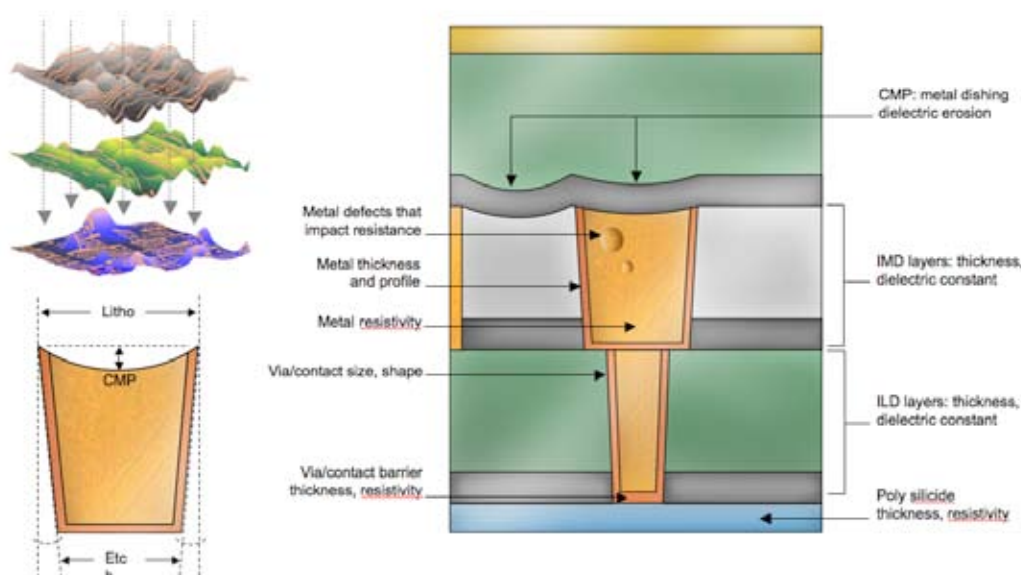


Figure 2: Multiple manufacturing effects challenge yield and performance

Lithographers deploy many creative methods to address the significant challenges of printing a 45nm half-pitch transistor gates with a stepper using a 193nm wavelength laser (see Figure 2). Immersion lithography, double patterning, and more sophisticated RET algorithms improve the control of polysilicon, metal, and contact features. Meanwhile, chip designers are employing both restricted and recommended design rules, yield-aware routing, increasingly sophisticated RET modeling, and critical area analysis to achieve better mask quality and higher yield.

Uneven planarity has a greater percentage impact at 45nm than at larger nodes because the metal height is less, and slight variations can significantly change electrical behavior. It even can cause short circuits if not enough metal is removed and “pooling” occurs across conductors. Because inconsistent metal leads to an uneven focal plane for the next layer’s lithography, designs need to account for inconsistent feature height as well as width. Etch modeling may similarly become critical at future nodes for predicting the post-etch interconnect geometry of the bottoms and sides of the conductors. While variations in metal thickness have been known to cause complete chip failures, the more widespread risk is uneven performance. Model-based algorithms for metal fill can improve the planarity of the wafer, so conductors in silicon are created as predicted. Also, extraction algorithms can incorporate planarity predictions to better predict timing.

Reliability and electromigration risk are exacerbated by the shrinking gate oxide and higher power and current densities in the 45nm process node. In particular, the shrinking gate oxide and higher power density will make negative bias temperature instabilities (NBTI) much worse. NBTI is accelerated by higher device temperatures which result from higher density designs, and by higher electrical fields which result from shrinking geometries with fixed voltage levels. Furthermore, NBTI is a tougher problem than most other reliability issues because it can cause immediate failures after burn-in yet exhibits a recovery effect which causes asymmetries in the aging process. The other traditional reliability concerns of device hot carrier injection (HCI) and interconnect electromigration (EM) also are getting worse in 45nm due to shrinking geometries and higher current density. However, HCI will only be problematic on peripheral logic because the 45nm core logic uses such small voltages. A holistic control panel approach would enable analysis, interpretation, and fixing of reliability and EM issues through one common environment that crosses platforms.

Historically, manufacturability was considered after design completion. However, the resulting production delays from cycles of error detection and correction or worse—re-spins—are not acceptable in today's competitive environment, in which meeting time-to-market and cost objectives is essential for success.

Cell libraries, custom IP, and variability-sensitive analog designs are key candidates for applying recommended design rules and manufacturing process models—if not on the entire chip, then at least on critical portions determined by the yield/area tradeoffs. Model-based approaches also can help compact the layout while increasing potential yield. Litho and CMP analysis also can aid the effective implementation of design intent. For example, where matched devices are required, model-based predictions aid layout designers so that the manufactured silicon behaves as expected.

It is often debated whether the yield gained by the DFM analysis compensates for the time spent in optimizing the layout. The more integrated the solution, and consistent the flags and fixes are, the less time it will take to achieve yield gain. It is also debated whether using one method for checking is rigorous enough. While cross checking by a second approach corroborates results, building the chip with an integrated approach increases productivity without eliminating the opportunity for extensive verification. The greatest yield, performance, and area improvements can be achieved in earlier design stages where designers have more control. The greatest leverage and efficacy of process-aware CAD tools comes from bringing process data into early planning, implementation, and coordination processes. Successful 45nm design benefits from a holistic approach to strategically incorporate yield, power, and performance improvements much earlier in the design cycle and throughout implementation and verification.

## SCALE AND COMPLEXITY

Increasingly, competitive designs such as multi-core processors include more and more transistors than last year's designs. The smaller transistor encourages a higher transistor count, because it costs less area than it did at larger nodes, and one effect is burgeoning design data to manipulate and store. Additional analysis to detect potential problems in performance and yield further increases the compute burden. (see *Figure 3*) These scale and complexity challenges require design tools with greater capacity, plus approaches like parallel computing, hierarchical analysis, and abstracts to edit and verify designs.

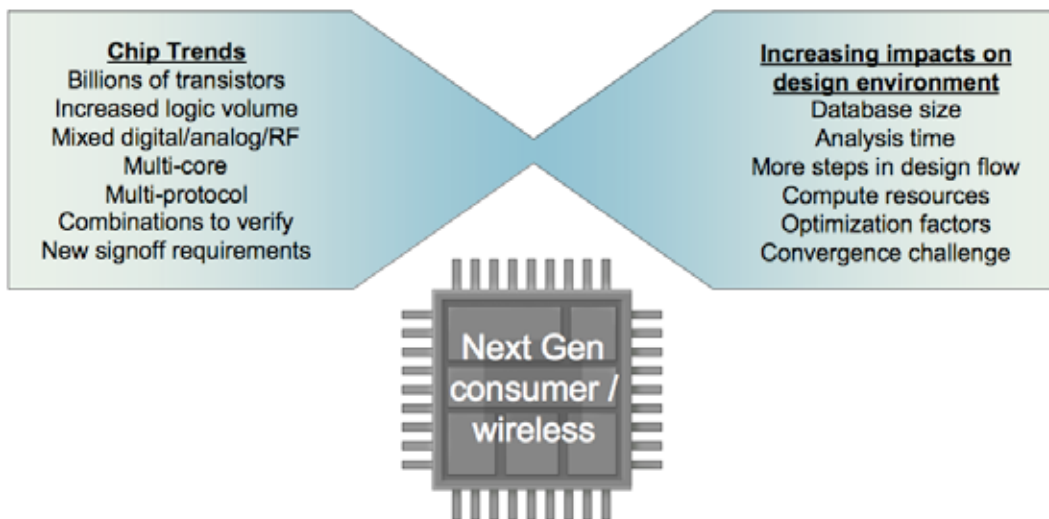


Figure 3: Chip trends and demands for more functionality increase scale and complexity.

While some aspects of increased complexity can be addressed through faster algorithms, distributed processing, multithreading, and faster hardware—with or without a holistic approach—optimization and productivity benefit from a complete integrated environment. Timing, routing, and DFM all require iterations of optimization. The top-level ability to abstract blocks and to selectively analyze units within the complete design reduces time spent in repeat runs. The complete flow acknowledges that an optimization for DFM may increase area or impair timing, thus requiring re-run. Integrated constraints protect against unintended skews to the existing design. Consistent techfiles and databases reduce time lost to overhead and enable more successful merger of custom and automatically-created layout.

## HOLISTIC APPROACH

---

Complete designs commonly include a combination of analog, custom IP, third-party IP, and automatic place-and-route digital blocks, all conceived and constructed separately. When assembled, a complete design benefits from a consistent infrastructure used on each component. Shared data formats reduce risks and surprises and save setup time. Integrated, shared databases provide the opportunity to make trade offs all at once or in a larger context. Innovations that let designers readily incorporate design rules, DFM models and guidelines, SPICE models, circuit design guidelines, voltage limits, device lists, and reliability models in a consistent manner, in all the steps that require them, would greatly help throughput and accuracy.

Design activities require information about the manufacturing process, and more sophisticated processes require more information from the foundries. As production processes mature, process information changes—design rules evolve, litho algorithms improve, even SPICE models vary—so convenient and secure updating of process information is necessary. However, more and more designs are happening in fabless or fab-lite environments where there may be less access to the manufacturing process information than in previous process nodes, and there is a growing drive for designers to have process-aware design solutions without being burdened with the manufacturing process details. Thus the methods for providing and updating process information are likely to evolve into increasingly automated infusion.

While sharing process information is one issue, there is also the challenge of protecting foundry IP so designers can get the data they need with minimal risk to foundries' proprietary knowledge. One approach for achieving this is the use of foundry-provided encrypted models that can translate the impact of process changes on the designed geometries without conveying explicit process changes.

Some manufacturability concerns can be handled more holistically by moving them upstream in the design flow. DFM checks and fixes can be applied to re-usable pieces of layout before they are used as part of a larger design. The advantage of this approach is that subsequent analysis and optimization can focus on only the routing layers. This methodology relies on good quality libraries and IP blocks, and it cannot accept significant post-layout modifications for risk of harming performance, as well as lengthening schedule.

Holistic chip design includes considering metal thickness limits and variability when planning power rails. Metal line maximum widths have shrunk due to CMP risks, and the narrow slotted metals have changed power distribution architecture. CMP modeling is used to predict the metal lines height and resulting resistance. For timing analysis CMP modeling is factored into the extraction calculations to report more predictive timing numbers. Someday the designer may choose to change the metal fill rather than the driver size or line length to meet timing. However a remaining challenge of modeling metal fill is for blocks placed repeatedly in different environments within the same chip. Different adjacent layout will produce a different result, and only an approach where all the data can be seen at once will give an informative analysis.

While the holistic approach begins with broad and thorough planning, summation of more focused integrations and new capacities add up to a fleshed out holistic flow. For example, low power circuits often use multi-supply voltages reduce power consumption without reducing functionality. While the approach is elegant, the validation is more challenging. Both crosstalk and delay calculations must be reviewed considering all the active voltages at once. Similarly, multi-mode simulation meets challenges at maturing stages of design, architectural, block level, and final full chip verification. The challenges of the new technology and scale manifest themselves in the day-to-day, designer-to-designer completion of new steps, handoffs, and iterations. The designers' productivity increases with tools targeted for these complex combinatorial approaches.

Complete designs often include parts built by hand requiring transistor-level analysis, along with parts built automatically that use gate-level analysis. While the goal of a smooth polished flow persists, the convergence of custom and automated blocks at the chip assembly stage currently requires management of different techfiles, and it generates a scattering of different kinds of data for potential yield improvement. DRC, CMP, litho, etch, and CAA all report out their own different flags for parts of layout that meet certain risk criteria. At least the results and flags could be made consistent. (see Figure 4) With consistent error reporting, algorithms could be applied to sort and prioritize risky layout. If each analysis is run separately, more time is invested interpreting error reports. Today interpreting and ranking error flags is done by experienced humans, but developing software to do it automatically in a foundry-approved manner will help both productivity and yield.

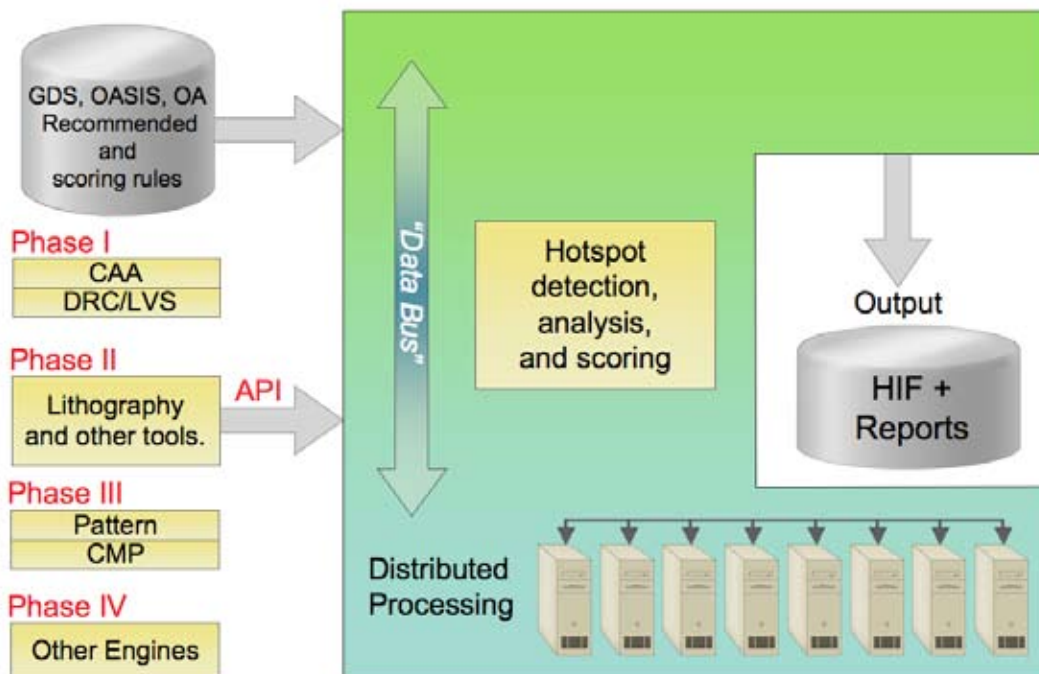


Figure 4: Multiple analysis technologies detect high-risk hot spots in the layout.

The daunting task of verifying, optimizing, and re-verifying whole chips is eased by the improving performance of verification software and is more effectively executed through planned hierarchy management. Hierarchy management saves time by identifying identical chunks of layout that are repeated throughout a design but can be certified just once. For some analyses, in subsequent instances of the same chunk, only the interconnect to the chunk needs to be verified. Reciprocally, there are checks that are run on identical chunks because they can be affected by the location and proximity to adjacent layout, and those especially benefit from running code where the mechanism for decreased runtime preserves the context of the data. The ideal 45nm holistic approach considers addressing challenges and opportunities of the smaller process node at the architectural level, and throughout the chip design process, including test and packaging. Manufacturing considerations are part of the floorplan and library building blocks. Scale and complexity are attacked through designing with abstracts, building a compute environment enabling intensive verification, and planning for integrated progression through a multi step design flow. While sign-off DFM will always be required, accounting for manufacturability, variability, and complexity at the beginning and throughout your chips' design cycle is the best way to produce competitive products that best utilize the advantages of 45nm processes.

A graphic consisting of a teal arrow pointing right, with a green gradient fill that tapers to a point on the right side.

For more information,  
log on to [www.cadence.com](http://www.cadence.com)

**cādence™**

**Cadence Design Systems, Inc.**

Corporate Headquarters  
2655 Seely Avenue  
San Jose, CA 95134  
800.746.6223 / 408.943.1234  
[www.cadence.com](http://www.cadence.com)