

CADENCE PALLADIUM XP VERIFICATION COMPUTING PLATFORM

Cadence® Palladium® XP is a state-of-the-art hardware/software verification computing platform. It unifies best-in-class simulation acceleration and emulation capabilities in a single environment to boost verification throughput and productivity. Its processor-based compute engine and Unified Xccelerator Emulator software runs high-performance verification applications and introduces flexible new use models that transcend traditional emulation. With unmatched scalability, advanced debug, hardware/software co-verification, and support for dynamic power analysis, hard and soft IP, and metric-driven verification, Palladium XP optimizes system design and verification.



Figure 1: Palladium XP offers a unified high-performance verification computing platform

SYSTEM-LEVEL VERIFICATION CHALLENGE

Traditional verification tools have not kept pace with the rapid rate at which system-on-chip (SoC) design size and complexity are growing. This widens the hardware/software (HW/SW) verification gap, limiting reusability and productivity and increasing the likelihood of re-spins and schedule delays. Traditional software simulators are ideal for IP or small design development and verification, and they can simulate cluster- to chip-level designs. However, as RTL design size increases, these simulators slow down significantly, which delays HW/SW (system) integration and prolongs the overall verification cycle.

As shown in Figure 2, today's SoC designs contain one or more micro-processors (uP), various types of memories, internal and external encrypted IP, industry-standard I/Os, embedded software, operating systems, drivers, and software applications that are interdependent; therefore, both hardware and software must be verified together.

As systems grow more complex, the risk associated with not adequately verifying HW/SW interaction also grows. Scalable performance is critical to eliminating these risks. Traditional hardware-assisted verification tools are useful for improving performance, but take you outside of your native simulation environment with steep learning curves, lengthy setup times, difficult debug methods, and reuse issues. Furthermore, there is no easy way to swap among simulation, simulation acceleration, and emulation environments without re-compilation.

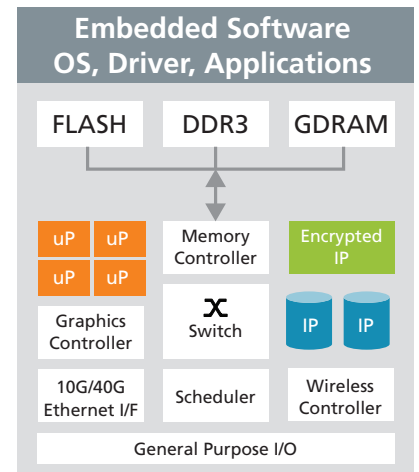


Figure 2: An example SoC design that includes hardware and software

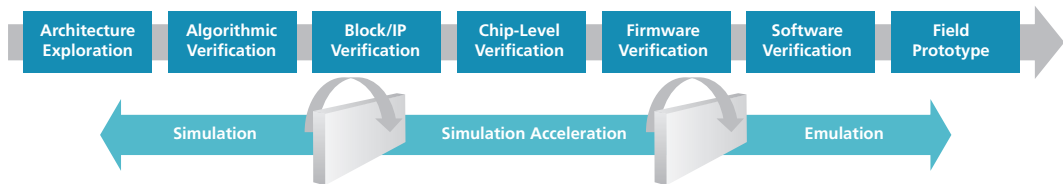


Figure 3: Disparate tools and segregated environments for simulation, simulation acceleration, and emulation create barriers to achieving scalable performance and IP reuse

SYSTEM-LEVEL VERIFICATION SOLUTION

To keep pace with the demands of advanced SoC development and to close the HW/SW verification gap, Palladium XP offers the industry's most comprehensive verification platform. Palladium XP removes the barrier to entry in acceleration and emulation by offering a unified environment that leverages the native simulation environment and allows a Cadence Incisive simulator user to hot-swap among simulation, simulation acceleration, and emulation environments at runtime without re-compilation. Palladium XP can be used at various design and verification phases, from early architectural analysis and block-, chip-, and system-level integration to software development and system verification.

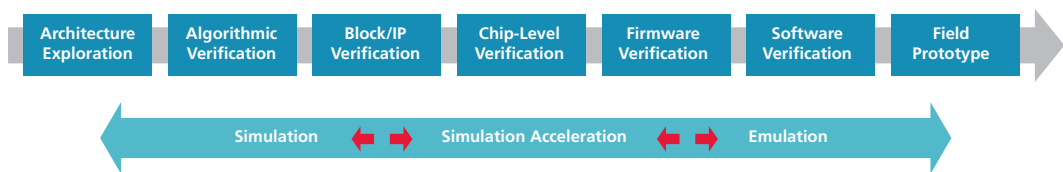


Figure 4: Palladium XP removes barriers to scalable performance with a unified flow and allows users to easily transition among simulation, simulation acceleration, and emulation

Furthermore, Palladium XP improves verification productivity by offering the fastest bring-up time, an easy-to-use flow, flexible simulation-like use models, scalable performance, and fast and predictable compile for the best turnaround time. It is designed to interface with real-world stimulus and enables hot-swap into the simulation environment while providing early access to HW/SW co-verification and advanced debug.

Palladium XP offers enhancements above and beyond what traditional acceleration and emulation use models offer. Palladium XP introduces new use models to improve verification productivity through metric-driven verification acceleration, hardware verification language-based testbench acceleration, Open Verification Methodology (OVM) acceleration, and system-level power verification.

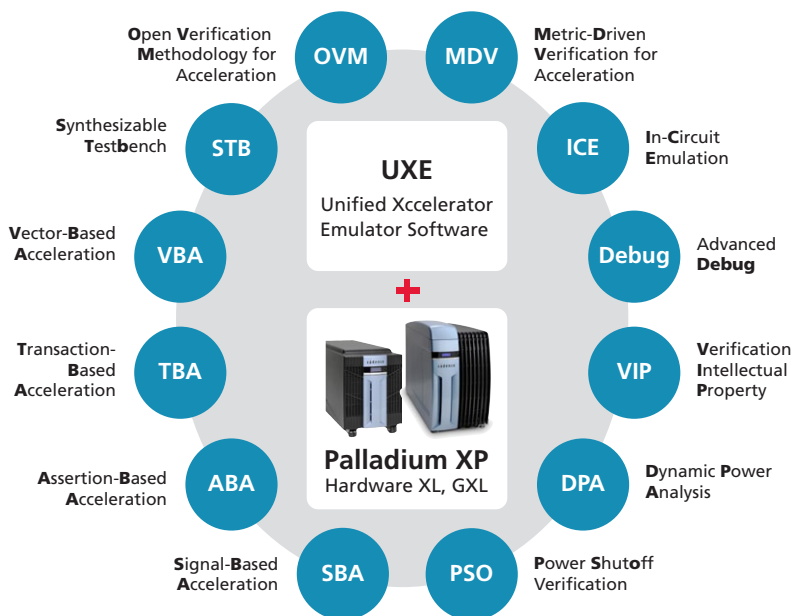


Figure 5: Palladium XP offers comprehensive use models for HW/SW co-verification and system realization

PALLADIUM XP BENEFITS

- **Highest scalability and flexibility**

- Enables centralized or locally distributed verification computing with scalable resources to serve a single user or as many as 512 simultaneous users for up to 2 billion gates capacity
- Supports flexible executable functional models at various abstraction levels (C/C++, SystemC®, instruction set or cycle accurate, silicon, RTL, gates)
- Offers flexible use models and flexible resource allocation

- **Unparalleled verification computing productivity**

- Integrates seamlessly with the simulation environment for multi-user productivity
- Facilitates best turnaround time with efficient compile, runtime performance of up to 4MHz, and simplified but superior at-speed and offline debug capabilities
- Reduces the learning curve with an easy-to-use flow, from simulation to acceleration to emulation, by leveraging the existing simulation environment

- **Better design bring-up predictability**

- Enables quick bring-up with its fast, automated, intelligent compiler that includes a rich set of behavior construct support and congruent (match) behavior between simulation and hardware
- Boosts runtime predictability with “hot-swap” to acceleration or emulation and the most flexible use models
- Enables quick system-level bring-up with comprehensive and proven Cadence SpeedBridge® portfolio (comprising hardware rate adapters for external targets)

- **Platform extension**

- Supports metric-driven verification for acceleration with coverage and advancements in hardware verification/hardware design languages
- Supports the most comprehensive hard or soft verification IP for standard protocols
- Enhances system-level low-power analysis with Dynamic Power Analysis option and power verification techniques such as power shutoff

PALLADIUM XP FEATURES

COMPREHENSIVE VERIFICATION COMPUTING PLATFORM

The Palladium XP verification computing platform is state-of-the art for its advancements in hardware, software (compilation, debug, runtime, flexibility), and use models. The Palladium XP compute engine comprises an advanced custom processor grid. Each processor includes multi-million transistors embedded in multi-chip modules (MCMs). This processor grid allows Palladium XP to support up to 2 billion ASIC gates of design capacity, supporting a single user or up to 512 simultaneous users, and it runs up to 4MHz. Its unique architecture enables high-performance verification for both small and large designs. Engineers can run their hardware and software verification tasks in parallel with cycle-accurate models while effortlessly migrating from a simulation environment to an acceleration/emulation environment.

The Unified Xccelerator Emulator (UXE) software component of Palladium XP integrates simulation and acceleration in a single environment, thereby enabling fast bring-up, superior debug, hot-swap capability, and fast, fully automated, predictable design compile on a single workstation. It is designed to support a large subset of behavioral RTL and enables efficient debug, thus increasing verification throughput and flexibility. For ease-of-use, UXE software makes the first-time user experience very similar to that of the simulation environment but with the speed of emulation.

FLEXIBLE RESOURCE ALLOCATION

Palladium XP offers verification computing resources with best-in class flexibility for an enterprise. It can be utilized for multiple projects/tests as it can support multiple concurrent jobs—including those with a mixture of acceleration and emulation—without affecting other jobs. Users can set up jobs queuing for regression or interactive use and can relocate jobs to other available symmetrically configured resources (MCMs, memories, I/Os) without re-compilation. Furthermore, users can respond to on-demand resource allocation requirements as projects needs evolve. Palladium XP offers the flexibility to make tradeoffs between maximizing runtime performance or maximizing capacity and the number of users.

FLEXIBLE MODEL SUPPORT

To assemble the SoC rapidly, at any given design phase, teams need to utilize the most accurate and highest performing models available. Therefore, a highly flexible verification platform is critical. The Palladium XP platform allows rapid integration of various abstracted IP models on the basis of performance, accuracy, availability, reuse, hard/soft IP, or legacy environment support requirements.

An ideal platform must also be able to leverage system behavior during emulation or acceleration to ensure models can be swapped in and out. To achieve these objectives, the platform must: (a) link to and co-execute with a high-performance “software-based” model (i.e., untimed functional models), and (b) link to and co-execute with a system-level interface and system-level components that are external (i.e., PCI Express or USB, program code running under diagnostic/firmware).

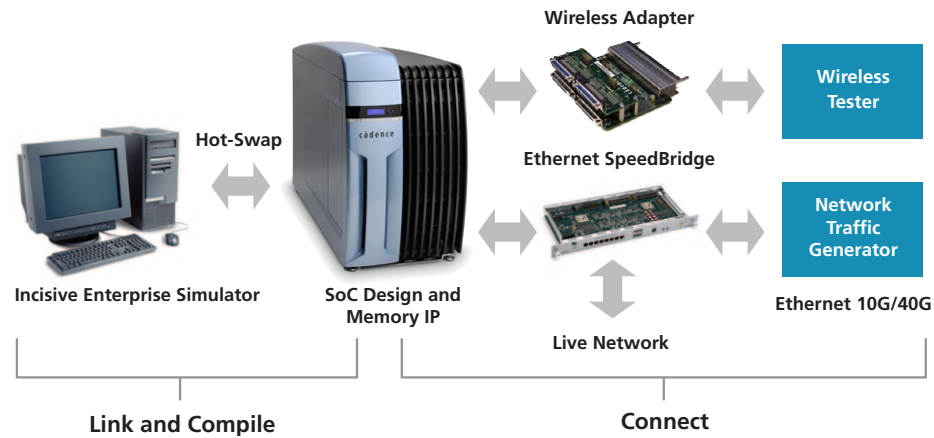


Figure 6: Palladium XP compiles/links to software models running on workstations and models compiled in hardware, and connects to real-world applications such as wireless testers and 10/40G Ethernet

Palladium XP simplifies the creation of system-level modeling by allowing different abstracted models to be compiled, linked, and operated upon. This unique capability enables users to rapidly create system-level models during the various design stages. By reusing models that are available in various abstracted levels (such as C/C++, SystemC, transaction-level models (TLMs), RTL, gate-level, and silicon-based IP), users can maximize reuse while balancing the need to verify the SoC model in a system-level context. In addition, Palladium XP supports industry interface standards such as the Standard Co-Emulation Modeling Interface (SCE-MI) or SystemVerilog DPI, which provides even more flexibility in expanding the system-level verification environment.

Since Palladium XP supports concurrent use of different types of IP, testers, debuggers, and test stimulus generators, it significantly reduces the development schedule. Users can comprehensively verify system interactions with a real-world environment and/or a testbench for a directed, constrained-random, or metric-driven verification environment while significantly improving verification throughput.

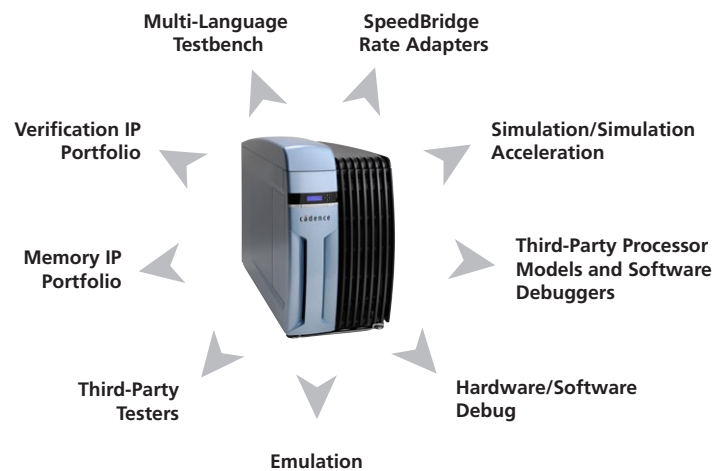


Figure 7: Palladium XP allows concurrent use of different types of models

FLEXIBLE RUNTIME ENVIRONMENT

The Palladium XP platform utilizes a high-performance runtime engine to enable acceleration of designs up to 4MHz. With its flexible Unified Xcellerator Emulator (UXE) software, Palladium XP offers tighter integration with the Incisive simulation and debug environment for simplicity and thus requires fewer interfaces between tools. It also supports metric-driven verification acceleration, provides a unified database for functional coverage to measure progress toward verification closure, and offers script compatibility with Incisive simulation and Tcl-based commands.

Users can dynamically and instantly swap, or “hot-swap,” the simulation state to and from acceleration and emulation—without re-starting the job—making Palladium XP flexible, efficient, and easy to use. With its hot-swap capabilities, Palladium XP leverages the software simulator to initialize unknown states, enabling the smoothest and fastest bring-up of design on hardware. Palladium XP simplifies use models to be simulation-like and embeds large subsets of non-synthesizable elements in hardware for flexibility. At runtime, users can have full visibility into their designs for debugging without sacrificing performance.

ADVANCED DEBUG


Palladium XP enhances the design debug process with its easy-to-use, high-performance debug features. To reduce the time and effort to locate the root-cause of an issue, it offers greater visibility into the design, the ability to trigger on events, conditional acquire, save snapshot and restore, and faster waveform upload. Palladium XP advanced debug also supports HW/SW co-verification and various assertions languages.

For visibility into the design, the FullVision feature ensures at-speed full visibility for any nets—up to 2 million samples for observation and analysis when used in a verification environment where the clock cannot be stopped due to protocol timeouts. Using dynamic probes, up to 20 million samples can be observed. Unlimited cycles of visibility are available when FullVision is employed in verification environments where the target clock can be started and stopped.

InfiniTrace enables unlimited trace capture depth and allows users to revert back to any checkpoint and restart emulation from that point. It also improves database preparation and waveform upload performance. Users can easily set up simple or complex triggers on sets of events and define or change runtime states with State Definition Language (SDL) without needing recompilation or impacting performance or capacity overhead.

Palladium XP offers a complete and central debug interface that can be controlled directly or managed through other verification environments. It offers longer and dedicated trace memory, conditional acquire capability with both FullVision and InfiniTrace, save and restore, and offline debug features to improve the user experience. For additional ease of use, the Palladium XP debug GUI transparently passes debug information to the integrated Incisive simulator and SimVision during run time.

Users can add probes to the hardware engine from the enhanced SimVision GUI, which can generate waveform databases in formats such as VCD, SST2, or FSDB for hardware debug. SimVision also allows engineers to control third-party embedded software debuggers in parallel with transaction- and signal-level hardware debug.



By linking to various third-party software debuggers, Palladium XP allows hot-swap to software simulation and interactive debug such as setting breakpoints or single stepping when running system applications. Palladium systems have already been tested with most third-party software development environments. In addition to supporting traditional JTAG connections to software development environments, Palladium XP interfaces with third-party environments (such as ARM processor models) through a virtual transaction-based environment to enable debug in a high-performance environment. With the Palladium XP debug interface, users have full visibility into HW/SW for co-verification in a system-level context.

SOLUTION EXTENSION AND ECOSYSTEM

HIGH-LEVEL SYNTHESIS WITH C-TO-SILICON COMPILER

UXE software can read RTL or gates created by Cadence C-to-Silicon Compiler to further accelerate verification early in the design cycle and enable HW/SW co-development with significantly less effort. C-to-Silicon Compiler automatically generates synthesizable RTL for both datapath and control functionality from timed and untimed C/C++/SystemC algorithm descriptions. Achieving quality of results at or above 90% of manual RTL design while also slashing engineering effort by up to 90%, C-to-Silicon Compiler bridges the gap between design complexity and efficiency of RTL code generation.

VERIFICATION IP AND IN-CIRCUIT EMULATION

The Palladium XP platform offers a variety of vertical, system-level design, and verification solutions with a broad ecosystem. In-circuit emulation (ICE) connects the Palladium XP emulator to a prototype of the system you're designing. Palladium XP typically replaces the ASIC(s) being designed for the target system, enabling system-level and application software testing prior to silicon availability. Unlike other systems, Palladium XP supports both static and dynamic targets, so it interfaces easily with virtually any target environment.

When interfacing with a real-world environment, it is sometimes necessary to control the relative timing of individual output signals from the emulator. Palladium XP provides direct support for all popular signal interfaces and has a vast number of I/O pins to support even the largest multi-user environments. Its UXE software can support HDL files encrypted by IP providers for protection, giving access only to the signals and registers permitted by that IP provider. Bonded-out microprocessor cores, silicon cores, or FPGA logic can be installed into the Palladium IP chassis using standard Cadence IP blocks, making it easy to utilize hard IP during verification.

Palladium XP is fully compatible with the complete family of Cadence SpeedBridge Adapters, providing simple and direct integration with full-speed in-circuit verification environments. Each SpeedBridge product is a transparent speed/rate adapter that connects real-world systems with the design being emulated. Palladium XP can also take advantage of recent software enhancements for controlling various functions through the GUI, such as soft reset of the board and remote configuration. SpeedBridge Adapters are an option to Palladium XP.



Figure 8: For most industry-standard protocols, off-the-shelf VIP such as SpeedBridge Adapters are available, enabling SoC designs running on Palladium XP to interface with real-world devices/targets/testers for system-level verification

TRANSACTION-BASED ACCELERATION

Transaction-based acceleration (TBA) is an optimized simulation acceleration mode that supports a transaction-oriented testbench modeling style. It accelerates logic simulation by several orders of magnitude. TBA uses message-level communication between the testbench components running on a workstation and the rest of the environment running on the Palladium XP platform. By using message-level communication rather than signal-level communication, TBA reduces the amount of communication overhead between the workstation and the emulator, thereby increasing overall acceleration performance.

- **Congruent TBA** allows users to create a transaction-based environment without using the hardware. Using only a simulator, such as Incisive Enterprise Simulator, engineers can fully develop their models and optimize environment bring-up time. Once the models are fully functional, engineers can then migrate painlessly to hardware, where these same models will run unchanged yet faster than with standard simulation. With congruent TBA, results are guaranteed to be the same, regardless of which engine (Incisive or Palladium XP) is employed.
- **Concurrent TBA** allows users to achieve near-emulation performance with designs being driven from a testbench. In this mode, the design runs continuously (free running) at full emulation speed while the testbench is running on the workstation. This unique feature is ideal for running large regression suites, where maximum performance is essential.

Palladium XP employs an Accellera standardized interface—SCE-MI—and SystemVerilog DPI to simulators with support for standard and advanced testbench languages, including SystemVerilog, SystemC, and C/C++.

HYBRID ENVIRONMENT

A hybrid of hardware and software verification IP (VIP) models can be used for increased predictability and productivity earlier in the design cycle. To complement TBA mode and further reduce design schedules, Cadence offers off-the-shelf VIP optimized for acceleration for various industry-standard protocols, as well as SpeedBridge Adapters optimized for emulation interfaces to various processor models, debuggers, and testers. Users can connect their VIP using a transaction-level modeling (TLM) interface and combine virtual prototyping with acceleration and emulation in a hybrid environment. The benefit of a hybrid environment is that users can achieve the best performance by leveraging available IP in the most flexible way.

AUTOMATED HW/SW CO-VERIFICATION WITH INCISIVE SOFTWARE EXTENSIONS

Incisive Software Extensions give your testbench access to embedded software exactly as if it were another part of the HDL design under test (DUT). Using extensions to the familiar Incisive SimVision debug tool, engineers can simultaneously control and verify software methods, procedures, variables, registers, and other elements with a traditional hardware-centric DUT using the same time-tested coverage-driven verification (CDV) process described in the Incisive Plan-to-Closure Methodology.

Furthermore, Incisive Software Extensions rise above HW/SW co-verification limitations by supporting processor models in any form: workstation-based host-code execution, Instruction Set Simulator (ISS), full RTL CPU models, hardware acceleration and emulation, and even prototype silicon. Incisive Software Extensions integrate with Palladium XP and are available as an option.

METRIC-DRIVEN VERIFICATION ACCELERATION

Palladium XP supports a metric-driven verification (MDV) flow, which enables users to follow a comprehensive plan-to-closure methodology that increases verification predictability, productivity, and quality. Verification plans are based on specifications; metrics are constructed with appropriate coverage, checks, assertions, and reuse.

By integrating with Incisive Enterprise Manager, Palladium XP can serve as a compute resource to help teams quickly determine when verification closure is achieved. Incisive Enterprise Manager automates and manages the execution of regressions on an accelerated verification compute platform. Users can more quickly measure and analyze progress toward signoff. Furthermore, by using a common verification plan (or vPlan), users can extract constraint results from multiple verification technologies (simulation, formal verification, simulation acceleration) into a common database for signoff analysis.

To simplify the adoption of metric-driven verification acceleration, Palladium XP also leverages the Cadence VIP portfolio.

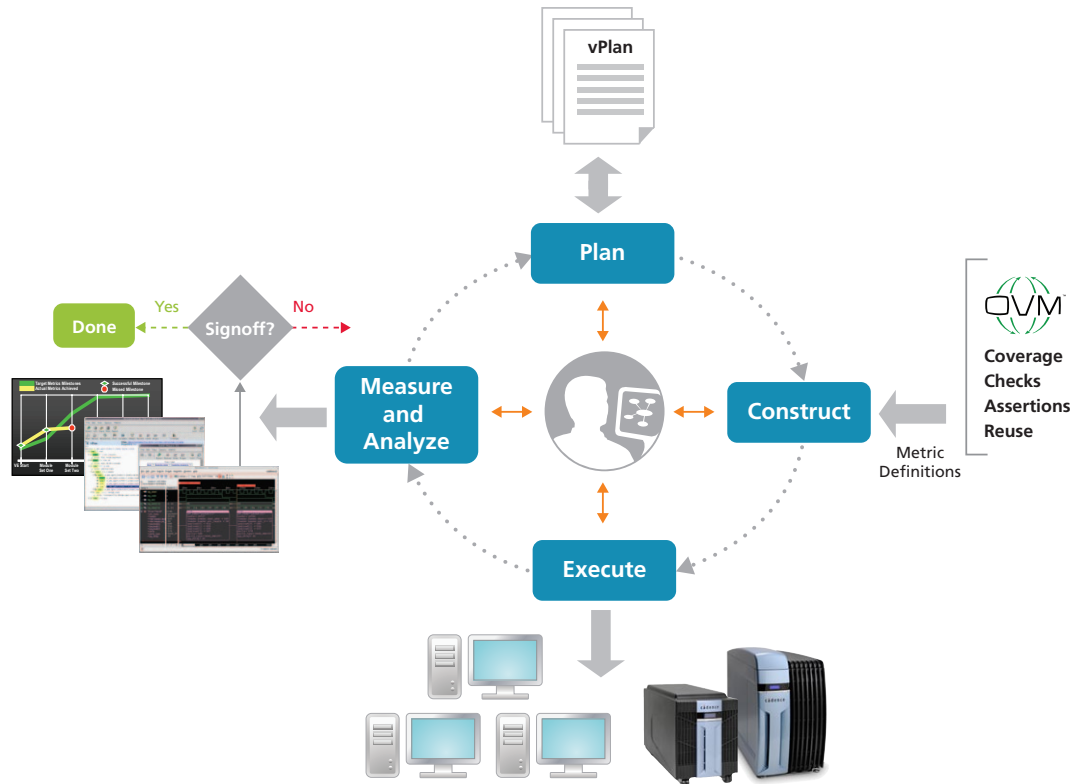


Figure 9: In an MDV flow, Palladium XP hardware executes the tests while its UXE software integrates with Incisive Enterprise Manager to measure progress

SYSTEM-LEVEL DYNAMIC POWER ANALYSIS

Traditionally, power analysis is performed using gate-level simulation and/or estimation based on spreadsheets from previous project estimations. The complexity of system-level SoC power analysis, however, requires better methods. Even for a modest SoC design, running it at 100MHz for 5 seconds equates to a duration of 500 million cycles. This may require a logic simulator to run for an entire week. Assuming you can run the simulator at speeds of about 100Hz, this can take weeks if not months on the workstation alone. Since power is also dependent on the application you are running, it is important to profile the power while running the application. Booting an OS and then running an application requires cycles that simulation alone cannot provide.

As shown in Figure 10, SoC power analysis requires “deep” cycles. Simulation users may focus their attention on a local peak, while emulation users can find a true peak during a long run under a specific condition that is not practical to produce in simulation alone. Palladium XP enables users to run additional cycles for system-level tests to find true power peaks and more realistic average power.

SoC Power Analysis Requires “Deep” Cycles (@100MHz for 5 seconds => 500 million cycles)

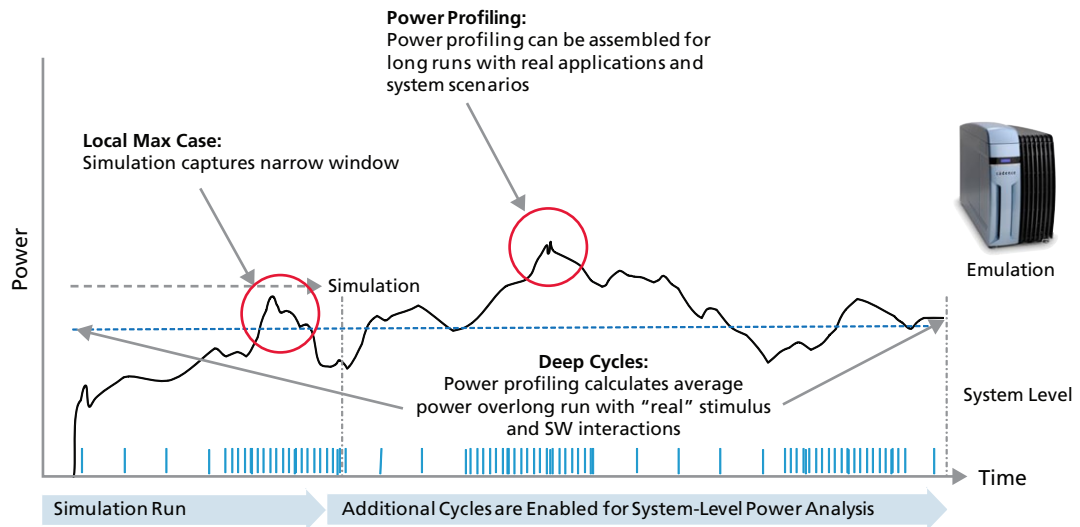


Figure 10: System-level power analysis requirements make it impractical for most users to rely solely on the simulator; the issue widens as core speeds of advanced SoCs push beyond 1GHz, requiring even deeper cycles for a small window of real-time analysis

The Palladium XP Dynamic Power Analysis (DPA) option represents a methodology shift for power budgeting of electronic devices with system-level implications. Using the high-performance Palladium XP engine, DPA enables users to run long system-level tests, empowering SoC teams to correlate the power consumption of a performance-sensitive function while preserving an acceptable user experience. DPA helps engineers quickly identify peak and average power of SoCs with “deep” software cycles (real-world stimuli) up to 4MHz throughput for RTL and gates due to switching activities. With Palladium XP built-in memory and the Cadence Encounter® RTL Compiler power estimation engine, Cadence provides the first high-performance, cycle-accurate, integrated solution delivering full-system power analysis of HW/SW designs.

With a successive-refinement approach, system designers can now make better decisions when selecting IP, an “adequate” package, and cooling requirements, and they can react quickly to changes in specification or environment. By testing against various operational scenarios and “what-if” analysis to make architecture tradeoffs, designers can make better decisions to save power. DPA is an option to Palladium XP.

SYSTEM-LEVEL POWER VERIFICATION

To reduce static power, when part of the device or IP (power domain) is not being operated, it can be turned off using techniques such as power shutoff (PSO), which can drastically reduce SoC power consumption. But with the use of PSO and other power reduction techniques, power verification complexity increases. The challenge is to ensure that the design continues to function as designed. For example, designers must verify that powered-off logic does not drive inputs to power-on parts of the logic, or that the sequence of power shutoff and power-on are implemented correctly.

For a larger design with multiple power domains, power verification may not be adequate with simulation alone due to performance limitations in the system-level environment. The Palladium XP high-performance engine with deep trace capability can be leveraged to verify power sequences at the system

level. Users can set up trigger conditions for power on/off and can use force operations to create low-power scenarios just as they would use them for functional verification during normal acceleration/emulation runs.

Palladium XP reads a common side file and helps designers verify power intent through the integrated SimVision waveform viewer and log file messages. Low-power verification capabilities are inherent to Palladium XP.

THIRD-PARTY SUPPORT

IP, MODELS, AND SOFTWARE

The Cadence IP Alliance Program enables interoperability and facilitates open collaboration among leading IP providers to build, validate, and deliver accurate models for Cadence design and verification solutions. It offers a broad and growing portfolio of world-class IP solutions paired with corresponding verification IP components in most cases. The Cadence Verification Alliance Program helps Cadence customers accelerate their adoption of new verification technologies and boosts their productivity.

TESTERS

To exercise (generate stimulus patterns) and to analyze protocol traffic patterns in a system-level environment, Palladium XP enables the use of various third-party testers supporting most industry-standard protocols. This helps verify protocol layers (full stack) while running software applications and debug issues.

SPECIFICATIONS

Palladium XP is available in two main configurations: XL and GXL. Both are RoHS compliant. They share a common architecture (MCM, memory cards, cables, software), providing the same functionality; however, they differ in physical characteristics and scalability requirements.

	Palladium XP (XL)	Palladium XP (GXL)
Scalable capacity and I/O	<ul style="list-style-type: none"> Capacity: Up to 32 million gates I/O: Up to 3,072 CMOS3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL 	<ul style="list-style-type: none"> Capacity: Up to 2 billion gates I/O: Up to 147,456 CMOS3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL
Default dedicated user memory	Up to 16 gigabytes	Up to 1 terabyte
Simultaneous users	From 1 to 8 users	From 1 to 512 users
Architecture	Custom advanced processors (MCMs)	
Design format and language support	<ul style="list-style-type: none"> HDL: RTL (VHDL, Verilog, SystemVerilog) and gate-level netlist HVL: C++, SystemC, Specman 'e', SystemVerilog, and Open Verification Methodology (OVM) acceleration Assertions: System Verilog Assertions (SVA), Property Specification Language (PSL), Incisive Assertion Library, and Open Verilog Library (OVL) 	
Memory transformation	Options for memory placement, compaction, squeezing, read port splitting, and merging	

	Palladium XP (XL)	Palladium XP (GXL)
HW/SW interfaces, connecting to third-party tools/IP/environment	<ul style="list-style-type: none"> • Various standards: SCE-MI 1.1/2.0 and TLM support • Most comprehensive SpeedBridge portfolio for standard protocols supporting most market segments • Application-specific interfaces: C/C++, PLI, VPI, SystemVerilog DPI, DPI-SystemC, VHPI, etc. and support for third-party interfaces to the standalone UXE model 	
Fast compile	Up to 35 million gates per hour with a single workstation for RTL	
Performance	Up to 4MHz, with built-in profiler that tunes performance for acceleration	
Advanced debug	<ul style="list-style-type: none"> • FullVision: see any signals with longer trace depth, unified database, tight integration with Incisive Enterprise Simulator and SimVision (up to 2 million samples) • Enables assertions and transaction viewing • InfiniTrace, hot-swap, triggers on simple to complex events, support for subset of system tasks • Dynamic probes and virtual probes with fast upload time (up to 20 million cycles) – superfast incremental upload, State Description Language (SDL) for hardware designers, integrated debug environment, and third-party SW debuggers and various hard/soft IP supporting HW/SW co-debug and co-verification • Power profile along with design signals in SimVision GUI 	
Flexible clocking	Supports a very large number of synchronous, asynchronous, and gated clocks	

WORKSTATION REQUIREMENTS

In addition to simulation acceleration connections to individual workstations, each Palladium XP system uses a host workstation. This host is connected via high-speed connection(s) over Fibre channel cable, handling the bulk data transfers to and from Palladium XP.

	Palladium XP (XL and GXL)	Number of users
Simulation acceleration communication channel	PCI Express slot x4	Up to 4 per channel – Up to 512
Palladium XP to host workstation	Fibre channel and Gigabit Ethernet through PCI Express slot x4	All users – Up to 512

Note: Host and acceleration workstation can be the same or different. It is not necessary to use the same workstations for host and simulation acceleration; this reduces CPU/memory requirements.

SUPPORTED WORKSTATIONS AND OPERATING SYSTEMS*

X86 INSTRUCTION SET ARCHITECTURE WORKSTATIONS

- OS type: Linux
 - RHEL 4, RHEL 5 (32-bit, 64-bit)
 - SuSE 10 (64-bit)

SPARC WORKSTATIONS

- OS type: Solaris
 - Solaris 10 (64-bit)

* Please check with your Cadence representative for the latest information and additional details as they are subject to change without notice.

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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