GLOBAL ROUTE ENVIRONMENT TECHNOLOGY FOR ALLEGRO PCB DESIGN GXL

Global Route Environment technology for Cadence® Allegro® PCB Design GXL sets the new standard in PCB design and layout. For the first time, PCB designers have an automated methodology and capabilities they need to capture design intent and utilize intelligent automation. This allows PCB designers to quickly solve challenges that previously would have taken hours of laborious work, threatening project schedules and budgets.

INTERCONNECT ENVIRONMENT

Today’s state-of-the-art, highly constrained, high-density designs—which typically are dominated by bussed interconnect—can take significant time to strategically plan and route. This is because traditional autorouting technology has not kept pace with the interface interconnect used on these designs nor is it able to adhere to a designer’s intent. Consequently, simply placing and autorouting these designs often fails to produce the desired routing results. Even with modern CAD technologies, PCB layout designers have relatively few intelligent tools to aid in the strategic planning and flow and routing of design interconnect. As PCB design complexity and size increases, dependence on manual tools and processes increases design cycle time, planning iterations, and workload. In order to effectively route these types of designs, the designers must begin interacting with an intelligent routing engine during strategic planning and placement and then continue to interact with the route engine throughout the design cycle—not simply to plan and route the board manually, as is often done today. To achieve the desired results, guidance needs to be provided to the router so it not only follows the design constraints but also follows good design practices.

Since the inception of CAD tools, PCB designers have sought an environment that would capture their design intent, provide decision feedback based on a global view of the design and then intelligently and automatically perform design tasks adhering to their design intent. Global Route
Environment technology establishes a new PCB design paradigm and represents a significant leap forward. It is the first solution of its kind to bring intelligent automation where no automation was previously available. Global Route Environment technology includes a new graphical interconnect flow planning architecture and a new hierarchically aware global routing engine.

![Figure 1: PCB design dominated by bussed interconnect.](image)

**BENEFITS**

- Intelligently plan and autoroute interconnect that could not previously be autorouted
- Capture all electrical constraints and designer intent
- Routing follows flow planning, resulting in a “correct the first time” execution
- Significant boost in performance and productivity
- Significant cycle time reductions during placement and routing
- Shortened overall design process in contrast to today’s manual planning and routing methods

**FEATURES**

**GRAPHICAL INTERCONNECT FLOW PLANNING ARCHITECTURE**

One of two key components of Global Route Environment technology is a graphical interconnect flow planning (IFP) architecture. IFP is an automated, graphical canvas to define, capture and validate a user’s design intent for strategically planning and flowing interconnect. IFP lets designers use their knowledge—in concert with the environment’s global view—to plan the best interconnect solution possible. This intelligent, automated methodology eliminates the need for manual planning of design interconnect.

Done graphically through abstraction of the interconnect data, IFP reduces design complexity by decreasing the number of design objects that must be managed. Busses and grouped interconnect are reduced to individual objects called Bundles. This abstracted data in the form of Bundles and Flows provides users with an easy to use, intuitive method to define and capture routing intent. This design intent includes routing paths, layers, and transitions. The design intent is validated against the environment’s understanding of the hierarchical relationships of all the interconnect in the design to all other interconnect, available space/density, available channels, topology, and constraints.
ABSTRACTION OF INTERCONNECT DATA

The problem of design data overload for the user is compounded by tools that don’t provide a way to conceptualize the problem, visualize it, or quickly assess whether a potential solution is good or bad—let alone resolve it. Interconnect flow planner enables designers to create intelligent abstractions of critical interfaces and capture interconnect design intent. Various levels of abstraction of the interconnect data to allow users to work with data that is more representative of how the connectivity and engineering teams visualize the data. This abstraction of interconnect data allows users to deal with connectivity in larger “chunks” or Bundles in the same way that users visualize the interconnect patterns and flows. For example, a DDRII bus or a PCI Express bus is made of a hierarchical set of interface bits with complex constraints. The Global Route Environment technology will create abstract representations of this data in the form of system or user-defined Bundles that can easily and intuitively be managed to capture a user’s design intent.
CREATION OF BUNDLES AND FLOWS

In order to accomplish the goal of defining, capturing, and validating a users design intent, Global Route Environment technology characterizes the interconnect data differently. The creation of Bundles allows the user to reduce design complexity by reducing the object count they are planning—going from fifty rats of an interface to five Bundles each composed of ten rats, for example. The content of design Bundles can be driven by three methods: logical aspects such as buses or group properties, physical aspects such as pin location, component placement, and grouping by user definition. Design Bundles can be refined and fine-tuned until the desired grouping is achieved. Without specific user intent, Bundles represent the most flexible level of abstraction and the system has the greatest flexibility in considering an interconnect solution.

Nonetheless, for large complex designs, the physical planning must go beyond the simple grouping of rats. Once designers impart explicit intent to Bundles, they are considered Flows and, as a result, trigger specific behavior from the system. Explicit intent can include the routing path to follow, layer selection and transition location, tuning types/location, and constraint refinement.

With specific design intent, the Flow graphic and system feedback will help with design interconnect planning. More importantly intent captured in the Flow will directly provide user intent to the router. Flows also allow the user to control layer transition areas. Along with allocating usable layers, the user can identify preferred areas to make layer transitions. Users can force layer transitions to occur by further refining Flow segments with individual layer assignments. By providing explicit interconnect flow guidance users can reduce the routing solution problem and yield significant performance improvements with the routing software as it adapts to levels of guidance from the user.

Figure 4: Flows now represent specific design intent, including X/Y guidance and desired layers.

HIERARCHICAL-AWARE GLOBAL ROUTING ENGINE

The second of two key components of the Global Route Environment technology is a hierarchically aware global routing engine. The global route engine’s algorithms are specifically designed and architected to understand the hierarchal relationship of all interconnect in the design to all other interconnect, available space/density, topology and constraints. The Global Route Environment technology creates a global view of design and routing constraints. The system uses this design intelligence to conceptualize the design, to make a hypothesis early in the process as to how nets need to be connected, to account for the impact of the first net as it relates to the last net, to determine the necessary space for all nets, and then to refine the initial hypothesis as it works through the solution with guidance from the designer. Prior to planning or routing, the route engine pre-plans all routing paths for all physical, spacing, and electrical constraints simultaneously.
The router has an inherent understanding of all available routing space and accounts for any routing object traversing a given area. This allows the designer to work with the router to plan complex bus interfaces, highly constrained net topologies, and dense component breakout, such as BGAs.

This global perspective of the design also makes it possible for the router to validate the user’s decisions and provide feedback throughout the planning and routing process. Together the designer and router build an interconnect solution before ever creating final detailed routing. The advantages to this flow/router-driven process is that all of the user’s design intent and constraints—both electrical and physical—are analyzed, evaluated, and planned early and concurrently throughout the entire process. This process is also superior for bus interface and “river” routing as the router understands the hierarchical dependencies and requirements. A significant performance boost in convergence can be realized since router thrashing is dramatically reduced. Because the router has a global view of the design, it understands the hierarchal relationships of all interconnect, and knows the available routing space.

![Initial plans lines representing the global router’s design intent feedback for X/Y guidance and desired layers.](image)

**Figure 5:** Initial plans lines representing the global router’s design intent feedback for X/Y guidance and desired layers.

**ROUTER-DRIVEN FEEDBACK MECHANISM**

The interaction of the graphical interconnect planning architecture and hierarchically aware global routing engine during the planning process gives designers the intelligent, automated tools needed to plan the best interconnect solution possible. Using router-driven feedback mechanisms that validate design intent, user’s can make intelligent decisions. Even if exact design intent or constraints is not known in the initial planning phases, Global Route Environment technology is a flexible planning environment. It can help the designer discover unknown interconnect issues early in the design by quickly analyzing intent and constraint trade-offs.

With multiple stages of routing analysis feedback on the feasibility of different interconnect proposals, performing “what if” studies and analysis provides multiple advantages over traditional, manual route planning studies. A typical problem to solve during route planning is the minimum layer requirements. Using a manual planning process designers must go through lengthy, time-consuming iterations of placement, routing, and layer assignments to decide on an optimal interconnect solution. Developing Bundles and Flows allows these same studies to be performed in a fraction of the manual planning time. Changing layer choices for Flows is a simple as a setting change, while layer changes for etch based studies requires copies across signal layers for a complete re-route. Bundles and Flows are dynamic objects that can adjust with changes and plan requests through the routing engine.
The Global Route Environment technology not only understands design intent, but can also help users to determine the correct and/or optimal solution spaces. Users have the option to work from an ambiguous design setup, through refinements to a final solution. Or, they may start at a very specific solution criteria and work backwards towards a less controlled specification until a desired solutions is realized.

![Figure 6: Refined plans lines representing the global router's design intent feedback for X/Y guidance and desired layers, which now includes tuning.](image)

**PLAN PERSISTENCY**

Even within a single design cycle, customers will gain efficiency by being able to back up to a previous planning phase—even from the final etch. A very common situation for this is the need to retune a bus/interface based on a constraint change late in the design cycle. Rather than re-route the etch, a user can backup to appropriate plan level and just move forward through router-driven planning process to automatically regenerate the etch solution to meet the new requirements. This is possible because Bundle and Flow planning information is embedded within the actual physical design and remains persistent in that file throughout the entire design cycle. The retention of this planning information can provide many efficiency gains for customer design cycles.

![Figure 7: Design interconnect represented by Bundles and Flows.](image)