

# Cadence Design IP: NAND Flash Controller

As storage moves away from traditional media, NAND Flash offers the mix of performance and cost required to support the latest applications. Controlling and interfacing with NAND Flash, however, poses a challenge when trying to maximize system-level performance. Cadence® Design IP for NAND Flash delivers the industry’s highest performance, most feature-rich, and most flexible NAND Flash solution that enables enterprise-class storage and embedded memory applications.

## Simplifying Flash Adoption

In an industry that lacks standardization in commands, timing, architecture, and even pin-out, NAND Flash is still being rapidly adopted for solid-state drives (SSDs), mobile drive applications, servers, and other computing and consumer applications.

Having worked extensively with Flash manufacturers to understand their device support requirements and trends, Cadence Design IP offers leading-edge performance and seamless support for all major NAND devices.

The Cadence NAND Flash Controller, combined with the Cadence NAND Flash Soft PHY, provides advanced capabilities for the latest NAND specifications. The Controller supports older legacy interfaces that are still widely used, and it provides unparalleled backward compatibility.

By hardware-accelerating many functions that are typically implemented in software, the Cadence NAND Flash Controller enables engineers to drastically improve performance while significantly reducing the integration effort.

## Key Features

- Universal Flash support across all vendors
- BCH error correction optimized for different applications
- Optional multi-level bit cell ECC ( 8, 16, 32, 64, and higher)
- Auto-detect and auto-config to reduce boot loader code generation
- Line-rate hardware detection and correction
- ONFI 1,2,3 and Toggle 1,2 device support
- Flash data width from 8 and 16 bits
- Asynchronous or synchronous mode
- Multiple low-power options
- Support for SLC and MLC boot operation
- Data and command DMA available
- Multi-plane operation
- Read/write cache command support
- Small data command support (partial page)
- Volume and LUN addressing
- Interlaced and NON-interlaced addressing

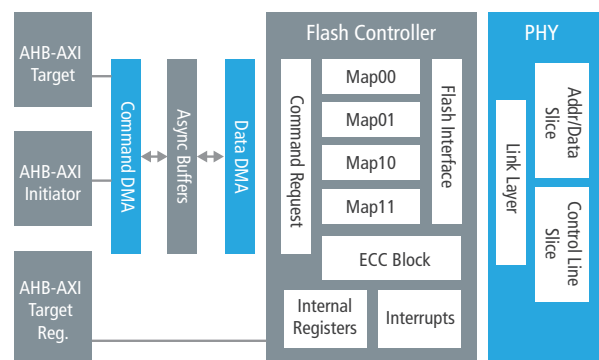


Figure 1: Cadence Design IP for NAND Flash offers a feature-rich and flexible solution

## Silicon-proven, scalable design IP

The Cadence NAND Flash Controller has been widely deployed across a range of applications and devices—without any silicon failures. Enabling so much hardware acceleration with so few issues demonstrates the robustness of the design in all silicon technologies, including FPGAs. And since Cadence Design IP offers a compliable approach to the Controller that supports a long list of configuration options, you get the exact controller you need for your design.

## Superior performance

The Cadence NAND Flash Controller has a performance-driven architecture that implements hardware acceleration for many functions typically done in firmware. Using the data and command DMA, the Controller can easily obtain within 10% of the theoretical maximum performance of the Flash device specification. For more random applications, the Controller supports partial page accesses.

## Advanced error detection and correction

Cadence takes a compliable approach to error code correction (ECC) that allows engineers to balance clock rates, buffer sizes, gate counts, and power. This flexibility, in turn, provides an optimized solution to the end customer. Options for correction include line rate, remote-based, 8/16 bit flash bus width, and custom ECC sectors.

Having multiple ECC solutions that are software-selectable supports numerous NAND cell technologies including single-level, multi-level, and triple-level cell (SLC/MLC/TLC). Advanced error detection and correction methods, including BCH and LDPC, future-proof your designs while improving reliability.

## Supported Interfaces

### Host

- Natively supports ARM® AHB™ and AXI™ master-slave 32/32 or 64/32
- Special applications are supported through a clean, low-latency FIFO interface

### Device

- Supports all major interfaces Asynchronous, ONFI, and Toggle
- High-performance or PHY link layers are supported by the Cadence DFI 2.0 NAND interface, modified so that customer-developed PHYs can be easily integrated

| Manufacturer     | Device Type | Comments  |
|------------------|-------------|---|
| Samsung          | SLC/MLC     | All known devices   |
| Toshiba          | SLC/MLC     | All known devices, logical block addressing (LBA) supported |
| Hynix            | SLC/MLC     | All known devices   |
| Micron           | SLC/MLC     | All known devices   |
| ONFI 1, 2.2, 3.0 | SLC/MLC     | All known devices mode 1-5                                  |
| Toggle 1, 2      | SLC/MLC     | All known devices 166MHz                                    |

Figure 2: Cadence Flash device support

## Deliverables

- Readable and commented RTL, fully regressed by Cadence for each customer delivery
- DFI 2.0 NAND modified pin description
- User guides and documentation
- Synthesis and STA scripts
- Basic testbench



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. [www.cadence.com](http://www.cadence.com)