

Cadence Design IP: NAND Flash Soft PHY

As storage moves away from traditional media, NAND Flash offers the mix of performance and cost required to support the latest applications. Controlling and interfacing with NAND Flash, however, poses a challenge when trying to maximize system-level performance. Cadence® Design IP for NAND Flash delivers the industry's highest performance, most feature-rich, and most flexible NAND Flash solution that enables enterprise-class storage and embedded memory applications.

Enabling High-Performance Flash Applications

High-speed NAND interfaces are rapidly being deployed in server and consumer applications. To realize the additional performance of NAND Flash requires using a PHY-based interface. The Cadence NAND Flash Soft PHY (second generation) provides a direct connection to the Cadence NAND Flash Controller using a NAND version of the industry-standard DFI interface. The PHY utilizes an all-digital DLL-based design to improve performance and reduce power consumption.

Offering complete support from asynchronous to ONFI 3 and Toggle 1,2 interfaces, the PHY is compatible with all major NAND devices. It includes a bypass mode to support legacy asynchronous devices within a single interface, and it is scalable from 1 to 24 8-bit channels. The PHY architecture is structured so that future clock rate increases can be easily accommodated.

Key Features

- Supports asynchronous, ONFI 1,2,3, and Toggle 1,2 devices
- Slice-based architecture
- Scalable from 1 to 24 channels.
- DFI 2.0 NAND modified interface
- Register interface for PHY programming

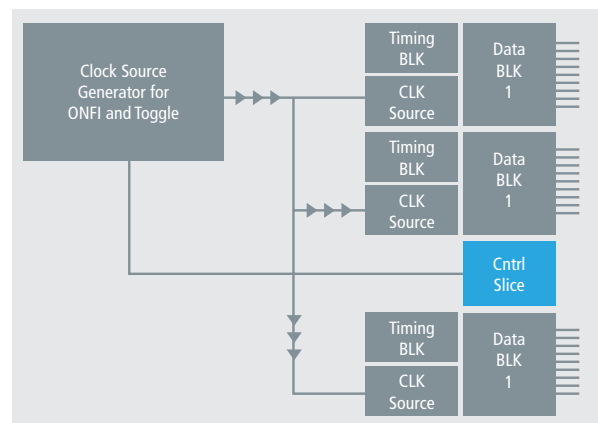


Figure 1: The Cadence NAND Flash Soft PHY is the industry's lowest latency solution, ensuring superior performance and power efficiency

- Integrated DLL supports speeds up to 300MHz (100MHz over current spec)
- Per-bit de-skew to handle shrinking read data valid window
- High-performance design using standard tool implementation flows
- Advanced test-mode capabilities

Silicon-proven, scalable design IP

The Cadence NAND Flash Soft PHY architecture is based on the proven Cadence DDR DRAM PHY design, and has been widely deployed across a range of silicon nodes.

Superior performance

The PHY architecture delivers the industry's lowest latency solution with superior timing, jitter, and lock capabilities.

Low power

Cadence DLL-based implementation of the PHY uses one-third the power of competitive offerings, significantly decreases gate counts, and permits operation at the Flash device frequency.

System integration

The DLL, the Controller, and the Flash interface run at the same clock frequency, which reduces the number of clock domains and reduces the clock frequency.

Unmatched flexibility

Using a very flexible slice-based approach for multiple channel support provides floorplan flexibility and simplifies layout. The ability to quickly achieve performance without special library cells, and to use standard tool implementation flows, result in faster time to market, lower cost, and optimal allocation of engineering resources.

Programmability

The Cadence NAND Flash Soft PHY uses a register-based control interface, adding to the robustness of the design for multiple layout requirements and devices. Configurable settings include:

- DLL settings
- Gate tuning
- DFT loopback control
- Programmable functional settings
- Programmable I/O settings

Supported Interfaces

Host

- SoC interface DFI with NAND modifications

Device

- Flash interface ONFI 1,2,3, Toggle 1,2, and Asynchronous support

Technology Support

ONFI 2,3	65nm and below LP, G*
Toggle 1,2	65nm and below*
Asynchronous, ONFI 1	Not required

**Hardening services are available.*

Deliverables

- Clear, readable, synthesizable RTL
- User guides and documentation
- Synthesis and STA scripts
- SDC constraints
- PHY layout guidelines
- Basic testbench
- DFI monitor
- Register configuration utility



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