

VeriSilicon and Cadence

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Steven Guo, Package Design and PCB Implementation Manager, VeriSilicon

The Customer

VeriSilicon Holdings Co. is a world-class IC design foundry that provides custom silicon solutions and system-on-chip (SoC) / system-in-package (SiP) turnkey services. The company’s solutions combine licensable digital signal processing cores, eDRAM, value-added mixed-signal IP, and other IP into SoC platforms that extends to sub-65nm process technologies. These platforms are used in a wide range of consumer electronics devices, including set-top boxes, home gateway devices, mobile Internet devices, cell phones, HDTV devices, and Blu-ray/DVD players.

For five consecutive years, Deloitte LLP has ranked VeriSilicon among the top 50 high-tech, high-growth companies in China. Red Herring named VeriSilicon one of the top 100 private companies in Asia, and EE Times named the company one of 60 emerging start-ups. Headquartered in Shanghai, China, VeriSilicon has R&D centers in both China and the United States, with sales and customer support offices throughout Asia, the United States, and Europe.

The Challenge

When VeriSilicon started working on an ASIC-based design that utilizes four Xilinx XC5VLX330-FF1760 FPGAs, the engineering team simply didn’t have time for a manual, error-prone process. To prototype the design within a limited cycle time, VeriSilicon needed an automated prototyping methodology and a robust verification platform that was both customizable and scalable.

To meet the project’s stringent requirements for timeline and quality, VeriSilicon turned to Cadence® Allegro® FPGA System Planner XL. This new-generation prototyping solution provides

Business Challenges

- Meet an aggressive timeline for an FPGA-based ASIC prototyping project
- Develop a scalable prototyping platform for hardware/software integration and co-verification

Design Challenges

- Accelerate the design process with automated, placement-aware pin assignment
- Optimize the physical connectivity, even as it changes
- Ensure quality and reduce complexity with reuse of interface rules and protocols

Cadence Solutions

- Allegro FPGA System Planner XL

Results

- Shortened the FPGA-based ASIC prototype development time by 75%
- Completed optimal pin assignment in one week vs. at least one month
- Achieved optimal physical connectivity for PCB layout
- Re-allocated FPGA banks and re-ran pin assignments easily and quickly

a platform to perform Verilog code porting, firmware and embedded operation system development, and system validation—and it helped the VeriSilicon design team complete pin assignment in just one week.

“With the growing complexity and scale of FPGA-based SoC verification for system board design, it’s a great challenge to shorten board bring-up time and ensure first-time-right design,” says Steven Guo, Package Design and PCB Implementation Manager, VeriSilicon. “With a traditional manual design methodology, it would have been impossible to meet the aggressive time-to-market requirements of this project. Using FPGA System Planner, we completed pin assignment in one week.”

“Allegro FPGA System Planner has many valuable features that helped us explore the FPGA-based architecture and create an optimum correct-by-construction pin assignment for the prototype design.”

Record Time for FPGA Design-In

With FPGA System Planner, VeriSilicon synthesized FPGA pin assignment based on user-specified, interface-based connectivity, FPGA device pin-assignment rules, and placement of FPGAs on the PCB. Automatic pin-assignment synthesis eliminated error-prone manual processes and shortened the time to create initial pin assignment.

“This placement-aware pin-assignment approach helped us greatly eliminate unnecessary physical design iterations and shorten our design cycle time,” Guo explains. “A manual pin-assignment process would have been error-prone, tedious, and time-consuming—it would have taken at least one month.”

VeriSilicon easily integrated the 1,000 pin-count FPGA on the PCB—from creating the initial pin assignment to automatically generating FPGA symbols and schematics to ensuring the device was routable on the board.

FPGA System Planner Features

The ability to handle design changes at any point during the design cycle is a key feature of FPGA System Planner. It was essential for the VeriSilicon design team to optimize pin selection for both FPGA and PCB requirements, and to automate symbol and schematic generation.

Guo’s team used the automated Cadence solution to define protocols between FPGAs and to specify rules for interface components to connect to the FPGAs. Next, they set proximity rules and ran pin-assignment synthesis to derive the connections of FPGAs and interface components. Once the connectivity was automatically synthesized, they generated symbols (or reused their corporate symbols) and schematics based on the synthesized connectivity.

By defining the protocols between FPGAs and the rules for interfacing to FPGA connectivity, Guo’s team worked at an interface and protocol abstraction instead of having to deal with thousands of FPGA pins. In a short time, the problems associated with complexity decreased by an order of magnitude. The Cadence methodology also enables design reuse—the interface rules and the protocols can be applied to other designs or used to optimize the same design multiple times. “We quickly developed a pin assignment and netlist with optimal physical connectivity for the PCB layout,” says Guo. “With Cadence technology, we were able to re-allocate FPGA banks and quickly and easily re-run pin assignments.”

FPGA System Planner also provided VeriSilicon with a “floorplan view” to place components in the FPGA system. This allowed the design team to specify connectivity between components within the FPGA sub-system at a higher level through interface definitions. “FPGA System Planner has many valuable features that helped us explore the FPGA-based architecture and create an optimum correct-by-construction pin assignment for the prototype design,” adds Guo.

Summary

Cadence helped VeriSilicon develop a flexible and robust ASIC prototyping platform for hardware/software co-verification and co-development—in record time. “We were able to shorten prototype board design time as well as bring-up time, eliminate unnecessary physical design iterations, and get to system validation in 25% of the time it would have taken us with traditional manual approaches,” Guo summarizes. “We will definitely continue to use Allegro FPGA System Planner XL.”



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com