



CADENCE AND TERADYNE

Teradyne Improves Productivity and Quality of Silicon Using Cadence Virtuoso Multi-Mode Simulation

“Virtuoso Multi-Mode Simulation has improved our ability to implement complex analog mixed-signal designs, ultimately helping us introduce higher quality end products to the market faster.”

Dominic Wong, Engineering Tools Strategy Manager, Teradyne, Inc.

CORPORATE PROFILE

- Teradyne is a leading supplier of automated test equipment for broadband communications, electronics assembly, semiconductors and automotive diagnostics

DESIGN CHALLENGE

- Complex analog and mixed-signal SoC simulations
- Wide variety of applications and test priorities

CADENCE SOLUTION

- Token-based licensing model for flexible simulation solutions over a wide range of design verification requirements
- Increased speed to market from a single testbench configuration directly integrated to the design process

CADENCE PRODUCTS AND SERVICES

- Cadence Virtuoso Multi-Mode Simulation
- Virtuoso UltraSim Full-chip Simulator, Virtuoso Spectre Circuit Simulator, and Virtuoso AMS Designer

MORE THAN A SINGLE CHIP

Based in North Reading, Massachusetts, Teradyne has been a leader in providing automatic test equipment (ATE) to component manufacturers since 1960. Today, it manufactures ATE systems for virtually every type of electronics, semiconductor and communications application for companies worldwide.

Each of these systems is designed with advanced custom chip sets. Teradyne wanted to implement a single, flexible methodology for use in its design and verification of complex mixed-signal SoCs, and across a wide range of other ICs. Several key considerations for Teradyne were simulation capacity for very complex analog mixed-signal designs and the ability to dynamically adapt to changing design priorities.

COMPREHENSIVE TEST CAPABILITY

Cadence answered Teradyne's substantial system-level requirements with the comprehensive Virtuoso® Multi-Mode Simulation solution. Virtuoso simulation technology provides designers with a complete design and verification environment for analog, RF, mixed-signal, memory and SoC designs. It combines the industry's leading SPICE, FastSPICE, RF and analog/mixed-signal simulators in a unique shared licensing package.

Teradyne has already used this platform in the successful development of an extremely complex mixed-signal SoC. The functional verification of this design required numerous individual simulations, building into a single complex full-chip simulation. Teradyne used Virtuoso Spectre Circuit Simulator and Virtuoso UltraSim Full-chip Simulator to design the analog blocks, allowing the team to implement a command-line mixed-signal verification flow with Virtuoso AMS Designer based on the same underlying analog solvers used during the analog block design. The transition from analog block design to mixed-signal verification was made easier by using the same underlying technology and model files as well as consistent results that were used during the block design and verification phase.

In order to manage the large number of complex, mixed-signal simulations required to verify this class of designs, Teradyne developed a logic verification design flow through top-level Verilog test benches. This change in perspective and methodology

has provided a significant positive impact on development schedules and final silicon quality.

Dominic Wong, Engineering Tools Strategy Manager at Teradyne, stated it like this, "We have an extremely complex mixed-signal SoC requiring a lot of mixed-signal simulations for functional verification of the design. Virtuoso Multi-Mode Simulation has helped us make our design flow more efficient by allowing us to use the simulator that we need, when we need it, ultimately leading to a shorter design cycle and better quality of silicon."

TOKEN-BASED VERIFICATION FLEXIBILITY

Not only are each of the products in this package leaders in their field, but Cadence's flexible token-based licensing allows Teradyne to use whatever subset of simulation technology they want at any given time, and change the mix whenever their needs change—without having to purchase the entire set of fixed licenses. This gives Teradyne a flexible advantage by allowing a shift in design simulation priorities dynamically. Leveraging the token-based model together with the capability that Virtuoso Multi-Mode Simulation provides to switch seamlessly between simulation engines allows the company to achieve shorter time to market with higher quality silicon and an optimized investment.

Wong affirmed, "Virtuoso Multi-Mode Simulation's combination of superior simulation technology and the flexible token-based licensing model increased the efficiency of our design flow, and maximized our return on investment. This enables us to build complex mixed-signal SoCs not only faster, but with higher quality as well."

The greatest impact that the adoption of the Virtuoso Multi-Mode Simulation package has had on Teradyne's design effort is not a single successful chip, but a fundamental change in the design and verification workflow, simulation capacity and overall methodology. Virtuoso Multi-Mode Simulation provides the complete solution for design and verification of analog mixed-signal SoCs in a consistent technology platform. By providing the complete solution, Cadence reduces the design cycle and rework costs.

That is why Teradyne has made Virtuoso Multi-Mode Simulation the core of their current major chip development projects. That kind of confidence comes from successful experience.

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Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 (*within US*)
+1.408.943.1234 (*outside US*)
F: +1.408.943.5001
www.cadence.com