

CADENCE AND TERABLAZE

ENCOUNTER RTL COMPILER ENABLES FASTER TIME TO QUALITY OF SILICON FOR COMPLEX ASIC DESIGN

TeraBlaze set out to create a next-generation switching architecture for the internet and enterprise networking markets. The resulting design was a complex multi-million-gate ASIC with timing and area challenges that their current synthesis tool could not handle. They were faced with the challenge of replacing a tool mid-stream in their design process.

"The Encounter RTL Compiler synthesis solution handled blocks of our design that the competition could not. The synthesis results we got gave us a much shorter timing closure process than we expected."

Shankar Mukherjee
President and CEO, TeraBlaze

CORPORATE PROFILE

- TeraBlaze develops smart silicon subsystem solutions for the internet and enterprise networking

DESIGN CHALLENGE

- Create a scalable data switch fabric with full-duplexed bandwidth of over 200 Gb/sec in TSMC 0.13 μ
- Find a synthesis solution that could handle the design's timing issues, encountered midstream in the design process

CADENCE SOLUTION

- Provided the Encounter™ RTL Compiler synthesis solution
- Met all timing closure challenges and improved area results

CADENCE PRODUCTS

- Encounter RTL Compiler synthesis solution

SWITCHING TECHNOLOGY THAT'S AHEAD OF THE CURVE

Over the past decade, we have seen the internet and enterprise networking industries grow from something of interest to a few to key enablers of the global economy. With that growth has come a need for innovation to allow infrastructure to keep pace with the demands of an "on demand" world.

Founded in 2000 in Cupertino, California, TeraBlaze develops silicon and subsystem solutions to address internet and enterprise networking challenges. They recognized that both of these industries had needs for solutions with maximum bandwidth and scalability. The team designed an architecture geared to the metro-internet market. The resulting product, Cashmere, was data switch fabric, scalable from 150 Gbps to 640 Gbps. It could provide 200 Gbps of full-duplex bandwidth at a smaller geometry than the competition.

The TeraBlaze team embarked on the design of Cashmere with a small, elite team of ASIC designers. They broke the 5-million-gate, 0.13 μ design into six large blocks. During the design implementation phase of the process, the team ran into problems with their synthesis tool. "When we began the design of Cashmere, we were not using Encounter RTL Compiler for synthesis," said Shankar Mukherjee, President and CEO of TeraBlaze. "Our design was very challenging, and our current tool was not able to handle the complexity."

A SMOOTH TRANSITION TO ENCOUNTER RTL COMPILER SYNTHESIS SOLUTION

Changing tools midstream in a design process can create significant issues. The new tool would need to achieve superior results while performing as part of an existing design flow. TeraBlaze chose the Encounter RTL Compiler synthesis solution for the task.

"Cashmere was designed to be a very high-bandwidth chip, so compile time was an important benchmark for us. We made the move to the Encounter RTL Compiler synthesis tool after meeting with their consulting team and learning about the tool's capabilities," continued Mukherjee. "The transition was very smooth. The tool plugged seamlessly into our design flow, and the consulting team remained on site to ensure that there were no issues."

ADVANCED SYNTHESIS TECHNOLOGY SHORTENS TIMING CLOSURE PROCESS

Encounter RTL Compiler delivers the fastest time to the highest quality of silicon. Getting better chip speed and smaller die size, after wires, in less time is of value to every design team.

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In addition, the Cadence synthesis solution delivered better results in area. "Having more margin before place and route made our ASIC handoff process much smoother," said Mukherjee.

Encounter RTL Compiler delivers global synthesis for timing closure. It uses a unique patented set of global focus algorithms that maximize the performance of challenging designs such as the TeraBlaze Cashmere design. The unique algorithmic technology dramatically improves critical path cell selection, overall library utilization, while still providing faster turn-around time and higher capacity.

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Shankar Mukherjee
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THE TOOL OF CHOICE FOR THE SECOND GENERATION

When TeraBlaze began development on their second-generation offering, a switch-on-a-chip product called Elan, there was no question about which synthesis technology they would employ. "We used Encounter RTL Compiler exclusively for development of our Elan product," said Mukherjee. "We have been very happy with the results from this tool, and with the support that we continue to receive."

Elan is designed to meet the needs of the enterprise LAN market, customers with more than double the bandwidth on less die size.

"Our goal is to provide the most advanced switching solution available for our customers," said Mukherjee. "It's important to us that we use the best products on the market to create our solution. With the Encounter RTL Compiler synthesis tool as part of our overall design process, we were able to meet our time-to-market window and deliver a superior, higher-value product to our customers."



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