SUCCESS STORY

# CADENCE AND RENESAS

## Cadence Encounter Timing System Helps Renesas Reduce "Pessimistic" Compensation in 65nm and Below Designs

"We performed rigorous evaluations of all commercially available statistical static timing analysis (SSTA) solutions that use comprehensive evaluation criteria. The SSTA technology in Cadence Encounter Timing System scored highest in our criteria for speed, accuracy, and timing optimization capabilities."

**Hisaharu Miwa,** *General Manager, Design Technology Division, LSI Product Technology Unit, Renesas Technology Corp.*

### CORPORATE PROFILE

- One of world's largest designers and manufacturers of LSIs and SoCs for mobile phone and automotive applications

### BUSINESS CHALLENGE

- Improve timing analysis methodology for better yield/ performance in 65nm and 45nm designs

### DESIGN CHALLENGES

- Process variation causes performance/ yield tradeoffs
- Implement SSTA without huge memory and processing time requirements

### CADENCE SOLUTION

- Encounter Timing System with SSTA
  - Very fast, accurate and does not require large work space
  - Tightly integrated with other Encounter capabilities

### CADENCE PRODUCTS AND SERVICES

- SoC Encounter™ GXL
- Encounter® Timing System GXL

## PESSIMISM A CRITICAL FACTOR

As each generation of chips moves to a smaller geometry, the line and gate dimensions of the circuitry strain the limits of manufacturability. Smaller circuits mean that tiny irregularities in the manufacturing process, called process variation, are closer to the acceptable tolerances for the basic functionality or failure of those circuits. Engineers must compensate for any potential weaknesses in their designs that could affect crosstalk, leakage. They must also compensate for the time it takes a signal to follow the myriad possible paths through the many millions of gates on a typical chip.

Given the competitive nature of the current electronics market, fabricating and testing the physical chip would be prohibitively expensive and time consuming. Engineers overcome this hurdle by creating software timing systems based on the individual characteristics of each component.

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Nevertheless, these virtual testing systems still have difficulty handling certain areas of the design and corner cases accurately, so engineers have to add conservative compensations in their calculations to improve the yield of chips that will meet the operating specifications.

However, such conservative or "pessimistic" assumptions also decrease the efficiency of the design. In fact, at 45nm geometries, the level of modification introduced by pessimism can be equal to or greater than the tolerance of the design. Clearly engineers need a new and more accurate timing system—one that can reduce the need for pessimistic compensation.

## BUILDING A BETTER DESIGN FLOW

Renesas Technology Corporation, a joint venture of Hitachi and Mitsubishi based in Tokyo, is one of the largest manufacturers of highly integrated SoCs. As Renesas recently began to design an engineering process for its next generation of chip development, the company was very concerned about timing analysis. The traditional method of static timing analysis (STA) began to show weaknesses that could not be ignored at advanced process nodes. With this in mind, Renesas decided to move to a statistical analysis and optimization solution, which would give them the ability to get a handle on the wide variety of process-related issues that can be devastating to the manufacturability and performance of advanced node designs.

"At advanced technology nodes, statistical timing analysis is necessary to eliminate over-design while maximizing performance," said Hisaharu Miwa, general manager of the Design Technology Division of the LSI Product Technology Unit at Renesas. "Improved modeling provides more accurate information to make critical trade-off decisions among performance, yield, and price."

In order to procure the best possible verification platform, Renesas decided to hold a competition. They invited the major test and verification system providers to their advanced research and design facility in Itami, Japan. The challenge they put to these providers was formidable: Develop a completely new, market-ready statistical static timing analysis (SSTA) product capable of covering a higher percentage of paths and corners—without requiring significantly more memory—and which could complete the task in less than 1.2x of the time it takes for a normal STA run.

The Cadence engineering team worked with the Renesas group to cover the hundreds of test cases involved in the evaluation. One of the key factors for success would be the ability to develop a library modeling and analysis scheme that covered a wider variety of the component combinations and interactions without growing the library to more than twice the size of a normal STA library.

In addition, Renesas had defined the three types of variations to be dealt with:

- Random variations on the chip that do not carry over to other areas or chips
- Distance-based variations that affect adjacent areas on a given chip design
- Global variations among complete chips

The only way to achieve all of these requirements at the same time was to tightly integrate a high-speed and accurate statistical timing engine into an industry proven design solution.

## CADENCE SURPASSES CRITERIA

Traditional STA adds in compensation for certain corner configurations and a "pessimism" fudge factor for process variation effects, which can be overly pessimistic. Alternatively, Cadence utilized its strength in static timing algorithms to develop a holistic and highly accurate block and path-level statistical analysis system that can be run in a single pass.

This provides a more dynamic understanding of the relative sensitivities to variation which results in faster processing, reduced margin, and quicker turnaround. When Renesas ran the final Cadence version against comprehensive evaluation criteria, Cadence was the clear winner in three important ways. The first achievement was accuracy, with Cadence meeting Renesas' rigorous criteria in over 95% of the paths. Cadence also exceeded the speed requirements by completing the 3.2 million-gate design verification in just 75% of the target run time. Thirdly, the SSTA technology from Cadence offered not just an isolated verification system, but also a tightly integrated solution with the industry-leading timing closure and sign-off capabilities of SoC Encounter GXL and Encounter Timing System GXL.

Miwa summarized the results as follows: "Over the course of nine months, we performed rigorous evaluations of all commercial SSTA solutions. The Cadence Encounter platform scored the highest in all of our criteria."

Renesas adopted Cadence Encounter Timing System with SSTA as its solution of choice for the backbone of its next generation of chip design and verification. This is the first time that a major developer has endorsed an SSTA timing optimization system.

The Cadence solution does not dramatically increase the workspace requirements, and can be easily deployed in a production environment workflow as part of a comprehensive development platform. The real benefits of SSTA include reduced risk of silicon failure, improved robustness and convergence of the design through a better understanding of tradeoffs, enhanced quality of silicon (QoS), significantly faster turnaround time, and a streamlined sign-off flow.

Cadence will continue to study and refine its implementation of SSTA through a close partnership with Renesas and other clients, as it prepares for the inevitable next step in shrinking geometries.

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